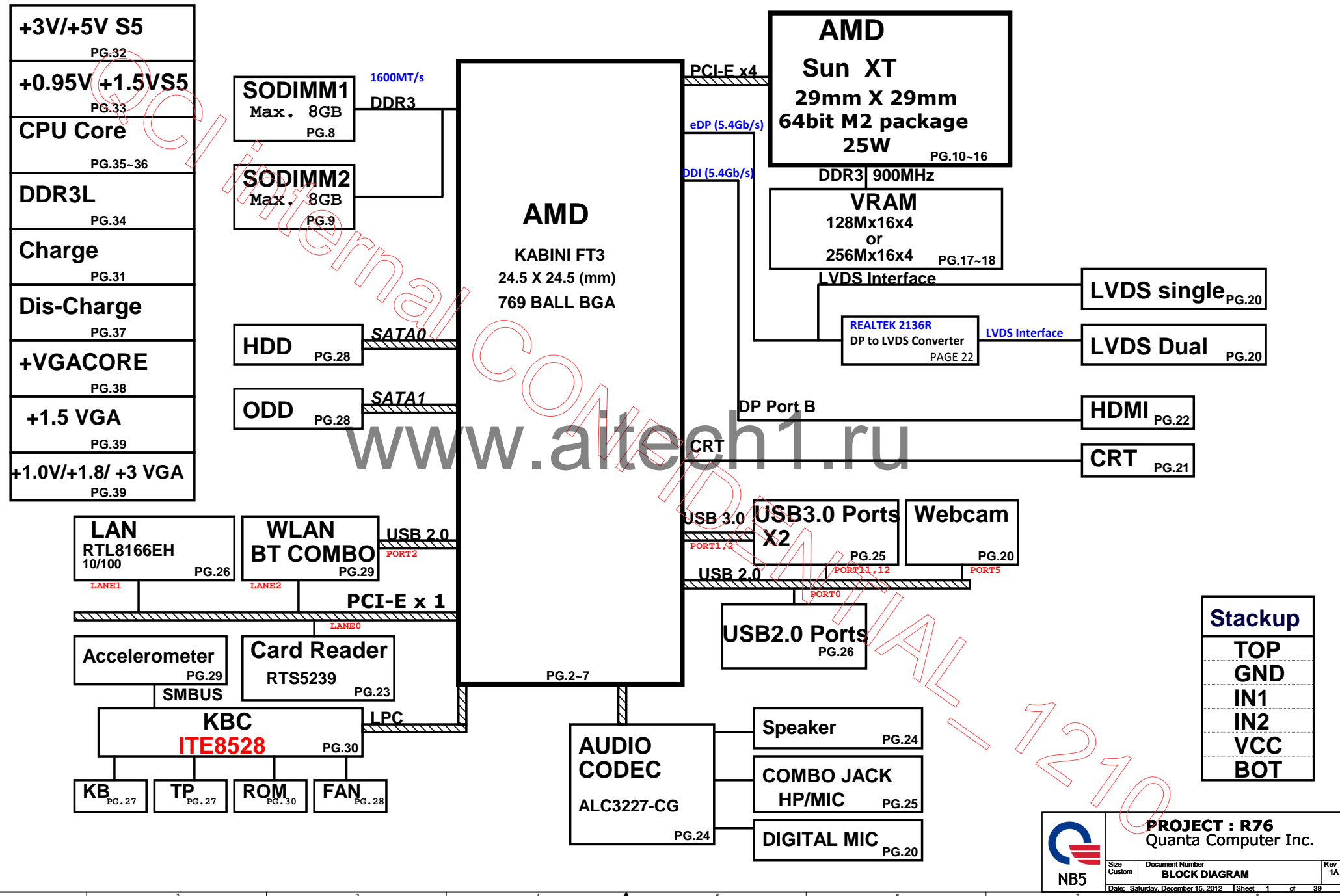
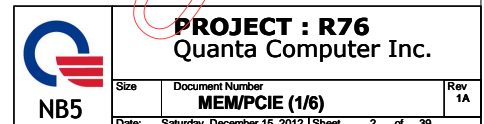
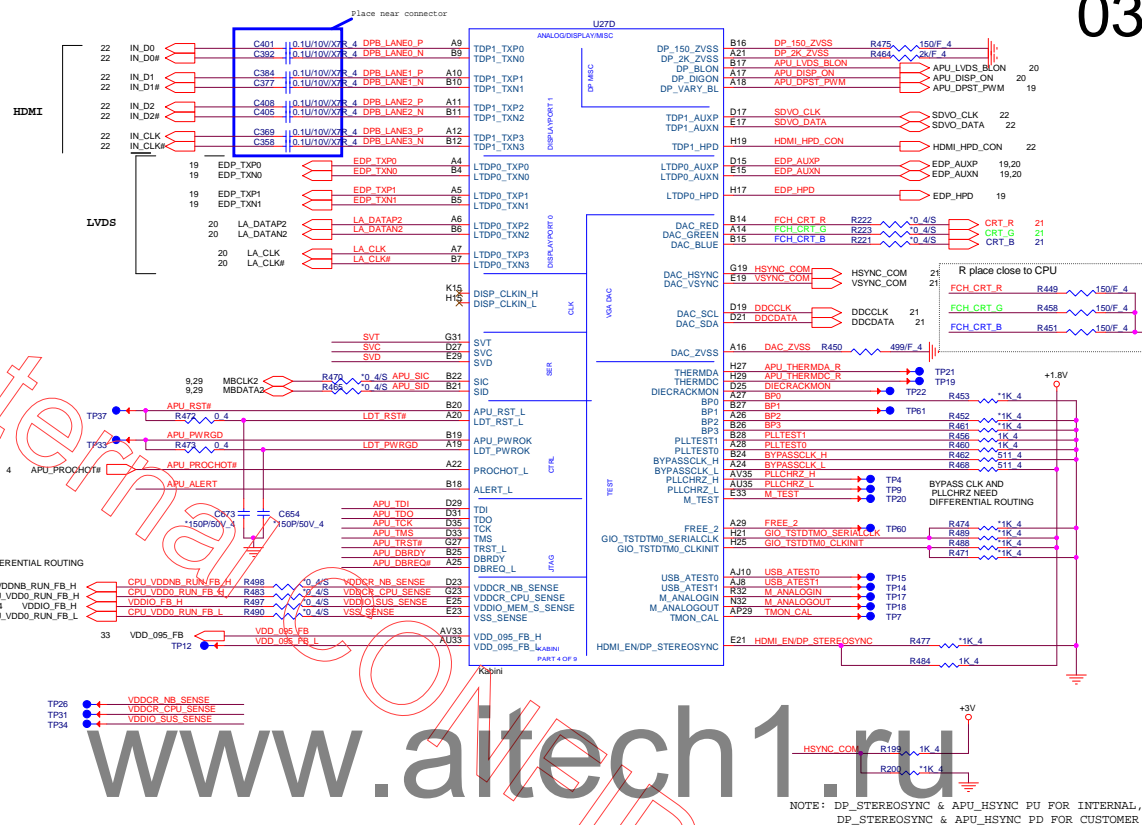
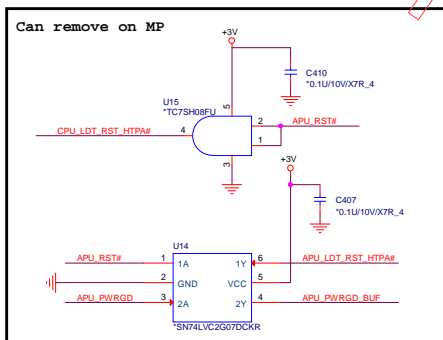
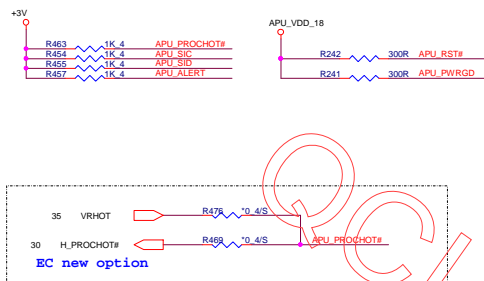


R76 AMD Kabini Platform Block Diagram

01



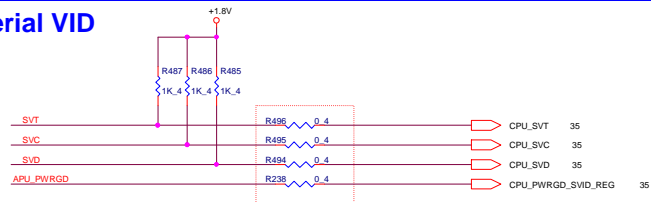




HDT(Hardware Debug Tool) Connector

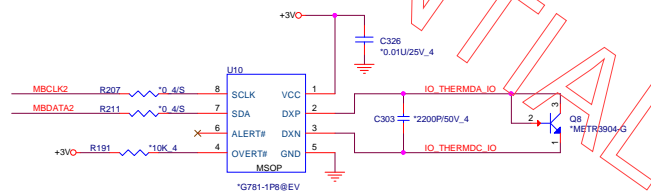


Serial VID

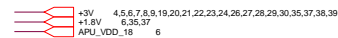


VFIX MODE		VID Override table (VDD)
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

Local Thermal Sensor



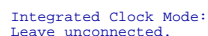
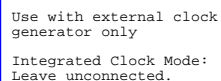
I2C ADDRESS: 9AH



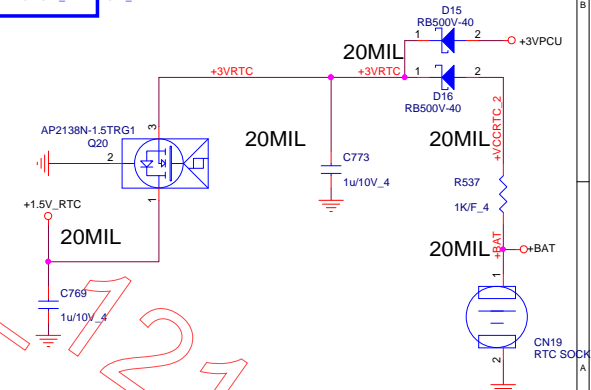
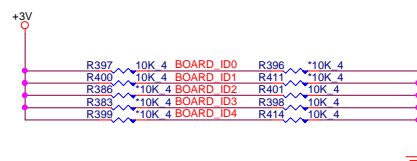
The schematic diagram illustrates the SPI interface for the MX25L1605DM21-12G memory device. The device is connected to a +3V5S supply and ground. The SPI_CLK signal is connected to pin 8 (VDD) of the memory device. The SPI_CS# signal is connected to pin 1 (CE#) of the memory device. The SPI_SO signal is connected to pin 5 (SCK) of the memory device. The SPI_SI signal is connected to pin 2 (SI) of the memory device. The SPI_HOLD signal is connected to pin 7 (HOLD#) of the memory device. The memory device is powered by +3V5S and grounded. The diagram also shows the connection of the SPI_CLK signal to the EMI filter and the SPI_HOLD signal to the +3V5S supply.

Components and connections shown in the diagram:

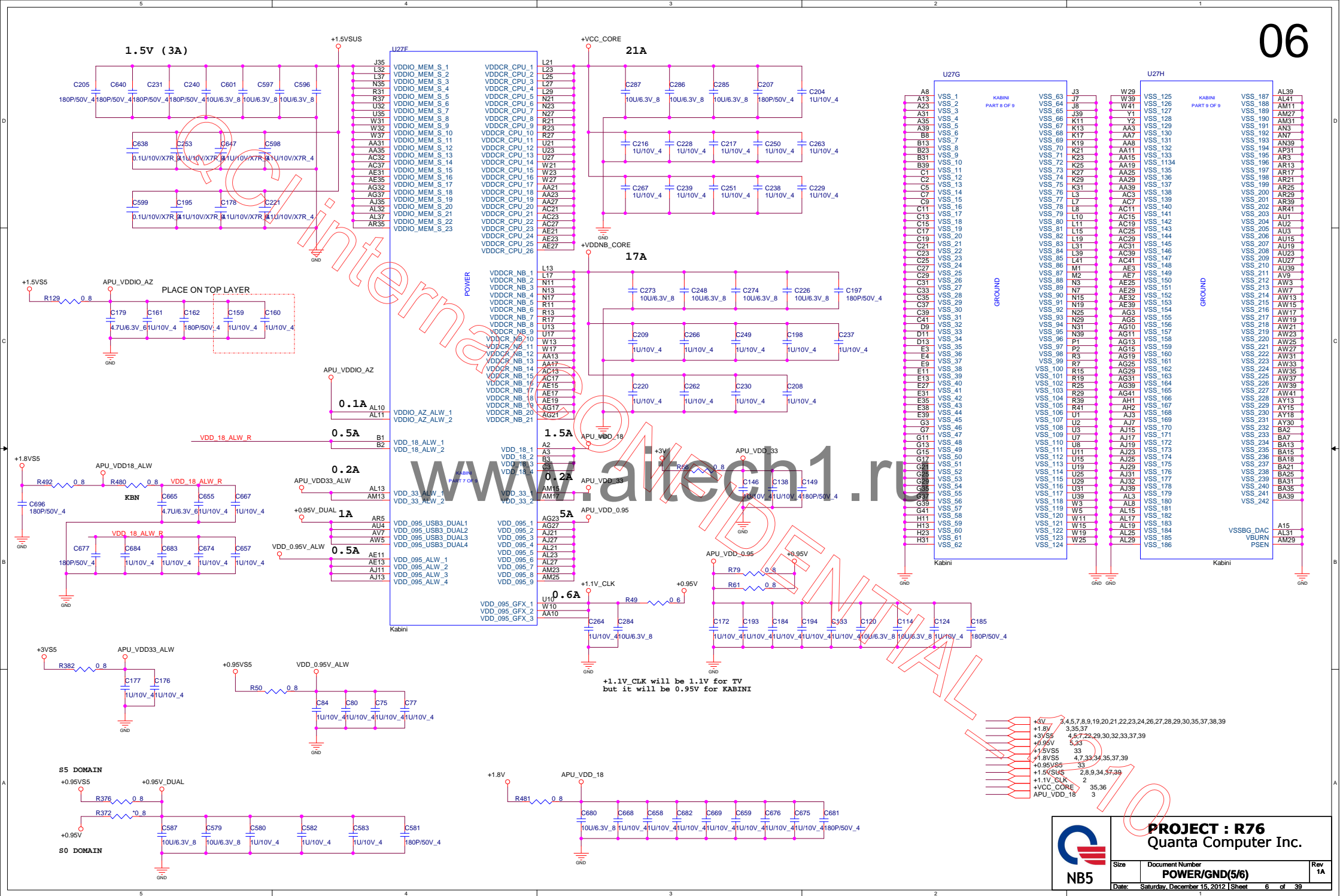
- Memory Device:** MX25L1605DM21-12G
- Power Supply:** +3V5S
- Ground:** GND
- Resistors:** R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R121, R122, R123, R124, R125, R126, R127, R128, R129, R130, R131, R132, R133, R134, R135, R136, R137, R138, R139, R140, R141, R142, R143, R144, R145, R146, R147, R148, R149, R150, R151, R152, R153, R154, R155, R156, R157, R158, R159, R160, R161, R162, R163, R164, R165, R166, R167, R168, R169, R170, R171, R172, R173, R174, R175, R176, R177, R178, R179, R180, R181, R182, R183, R184, R185, R186, R187, R188, R189, R190, R191, R192, R193, R194, R195, R196, R197, R198, R199, R200, R201, R202, R203, R204, R205, R206, R207, R208, R209, R210, R211, R212, R213, R214, R215, R216, R217, R218, R219, R220, R221, R222, R223, R224, R225, R226, R227, R228, R229, R230, R231, R232, R233, R234, R235, R236, R237, R238, R239, R240, R241, R242, R243, R244, R245, R246, R247, R248, R249, R250, R251, R252, R253, R254, R255, R256, R257, R258, R259, R260, R261, R262, R263, R264, R265, R266, R267, R268, R269, R270, R271, R272, R273, R274, R275, R276, R277, R278, R279, R280, R281, R282, R283, R284, R285, R286, R287, R288, R289, R290, R291, R292, R293, R294, R295, R296, R297, R298, R299, R300, R301, R302, R303, R304, R305, R306, R307, R308, R309, R310, R311, R312, R313, R314, R315, R316, R317, R318, R319, R320, R321, R322, R323, R324, R325, R326, R327, R328, R329, R330, R331, R332, R333, R334, R335, R336, R337, R338, R339, R340, R341, R342, R343, R344, R345, R346, R347, R348, R349, R350, R351, R352, R353, R354, R355, R356, R357, R358, R359, R360, R361, R362, R363, R364, R365, R366, R367, R368, R369, R370, R371, R372, R373, R374, R375, R376, R377, R378, R379, R380, R381, R382, R383, R384, R385, R386, R387, R388, R389, R390, R391, R392, R393, R394, R395, R396, R397, R398, R399, R400, R401, R402, R403, R404, R405, R406, R407, R408, R409, R410, R411, R412, R413, R414, R415, R416, R417, R418, R419, R420, R421, R422, R423, R424, R425, R426, R427, R428, R429, R430, R431, R432, R433, R434, R435, R436, R437, R438, R439, R440, R441, R442, R443, R444, R445, R446, R447, R448, R449, R450, R451, R452, R453, R454, R455, R456, R457, R458, R459, R460, R461, R462, R463, R464, R465, R466, R467, R468, R469, R470, R471, R472, R473, R474, R475, R476, R477, R478, R479, R480, R481, R482, R483, R484, R485, R486, R487, R488, R489, R490, R491, R492, R493, R494, R495, R496, R497, R498, R499, R500, R501, R502, R503, R504, R505, R506, R507, R508, R509, R510, R511, R512, R513, R514, R515, R516, R517, R518, R519, R520, R521, R522, R523, R524, R525, R526, R527, R528, R529, R530, R531, R532, R533, R534, R535, R536, R537, R538, R539, R540, R541, R542, R543, R544, R545, R546, R547, R548, R549, R550, R551, R552, R553, R554, R555, R556, R557, R558, R559, R560, R561, R562, R563, R564, R565, R566, R567, R568, R569, R570, R571, R572, R573, R574, R575, R576, R577, R578, R579, R580, R581, R582, R583, R584, R585, R586, R587, R588, R589, R590, R591, R592, R593, R594, R595, R596, R597, R598, R599, R600, R601, R602, R603, R604, R605, R606, R607, R608, R609, R610, R611, R612, R613, R614, R615, R616, R617, R618, R619, R620, R621, R622, R623, R624, R625, R626, R627, R628, R629, R630, R631, R632, R633, R634, R635, R636, R637, R638, R639, R640, R641, R642, R643, R644, R645, R646, R647, R648, R649, R650, R651, R652, R653, R654, R655, R656, R657, R658, R659, R660, R661, R662, R663, R664, R665, R666, R667, R668, R669, R670, R671, R672, R673, R674, R675, R676, R677, R678, R679, R680, R681, R682, R683, R684, R685, R686, R687, R688, R689, R690, R691, R692, R693, R694, R695, R696, R697, R698, R699, R700, R701, R702, R703, R704, R705, R706, R707, R708, R709, R710, R711, R712, R713, R714, R715, R716, R717, R718, R719, R720, R721, R722, R723, R724, R725, R726, R727, R728, R729, R730, R731, R732, R733, R734, R735, R736, R737, R738, R739, R740, R741, R742, R743, R744, R745, R746, R747, R748, R749, R750, R751, R752, R753, R754, R755, R756, R757, R758, R759, R760, R761, R762, R763, R764, R765, R766, R767, R768, R769, R770, R771, R772, R773, R774, R775, R776, R777, R778, R779, R780, R781, R782, R783, R784, R785, R786, R787, R788, R789, R790, R791, R792, R793, R794, R795, R796, R797, R798, R799, R800, R801, R802, R803, R804



Model	BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	BOARD_ID4
15" UMA	0	0	0	0	0
17" UMA	0	1	0	0	0
15" DIS	1	0	0	0	0
17" DIS	1	1	0	0	0

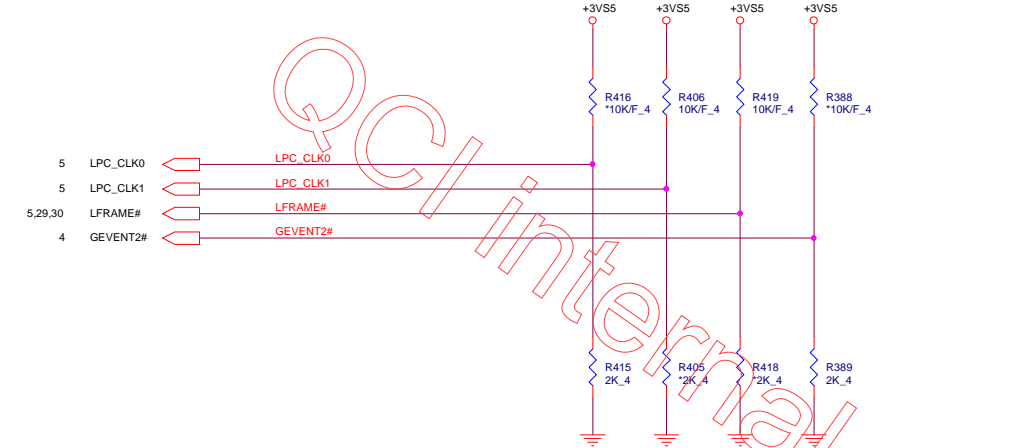


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Date:	Saturday, December 15, 2012	Sheet	5 of 39



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

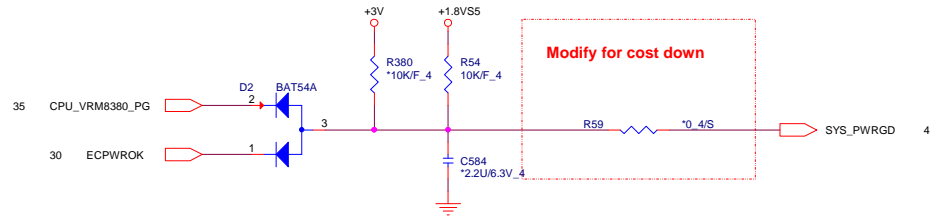


REQUIRED STRAPS

					LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH					BOOT FAIL TIMER ENABLED	CLKGEN ENABLED	SPI ROM	1.8V SPI ROM
PULL LOW					BOOT FAIL TIMER DISABLED	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM

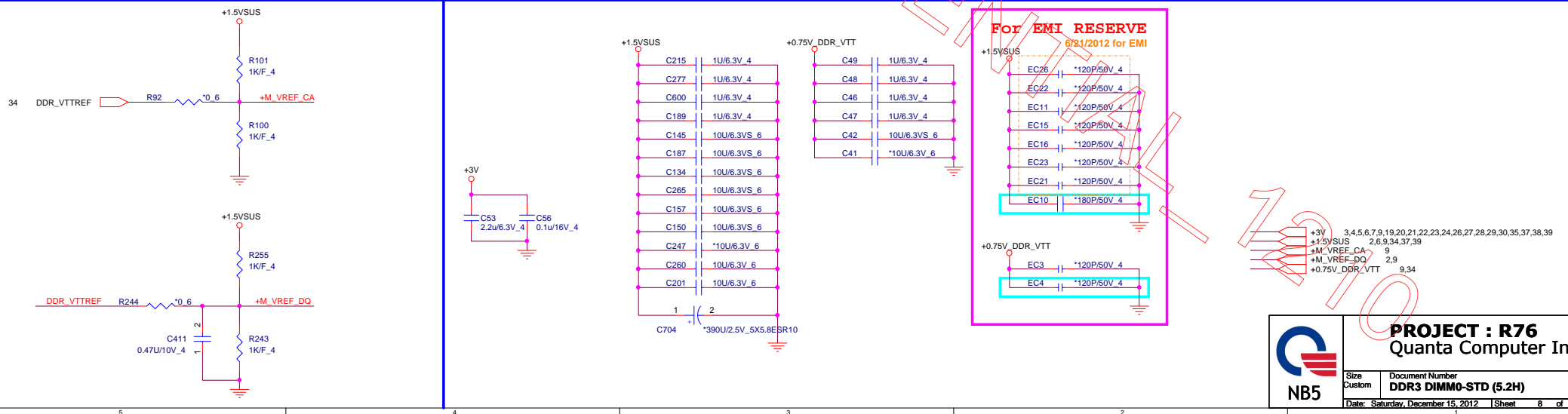
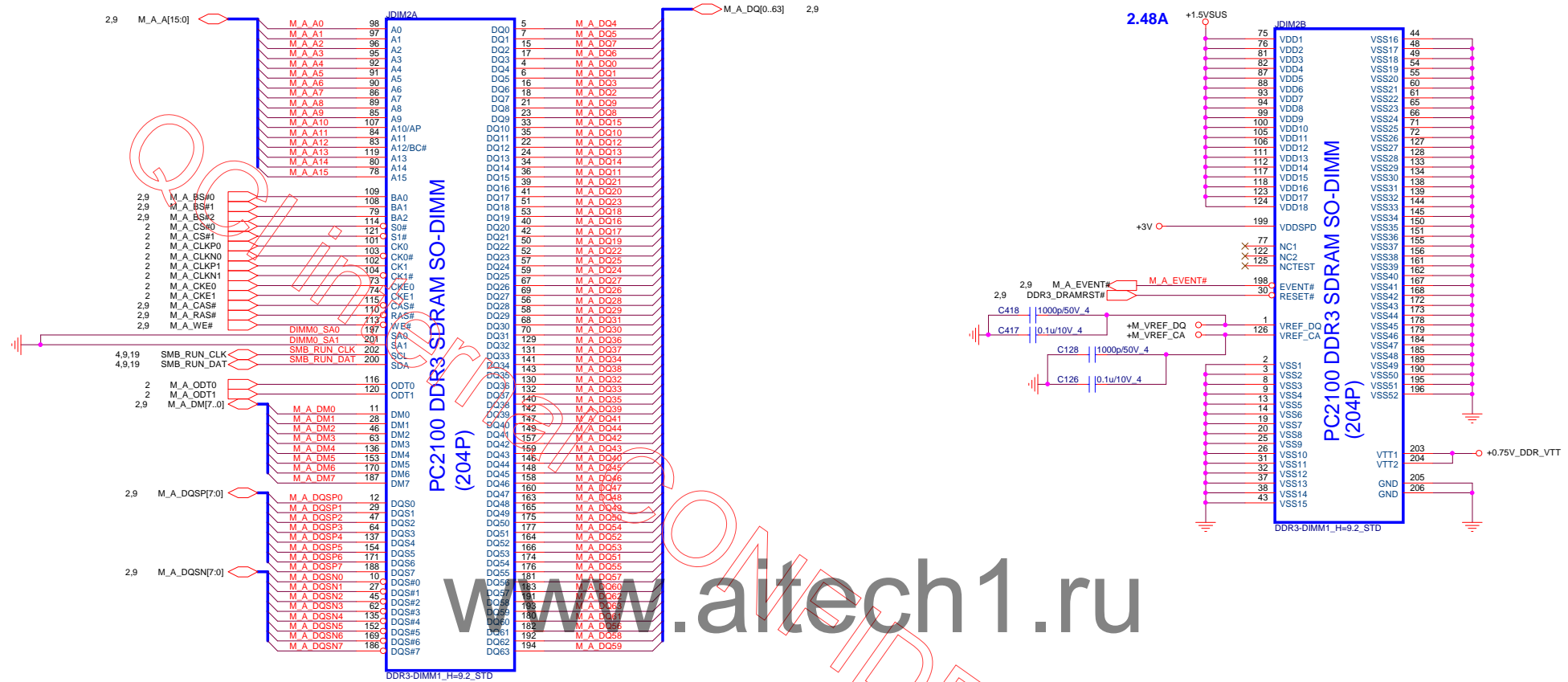
DEBUG STRAPS

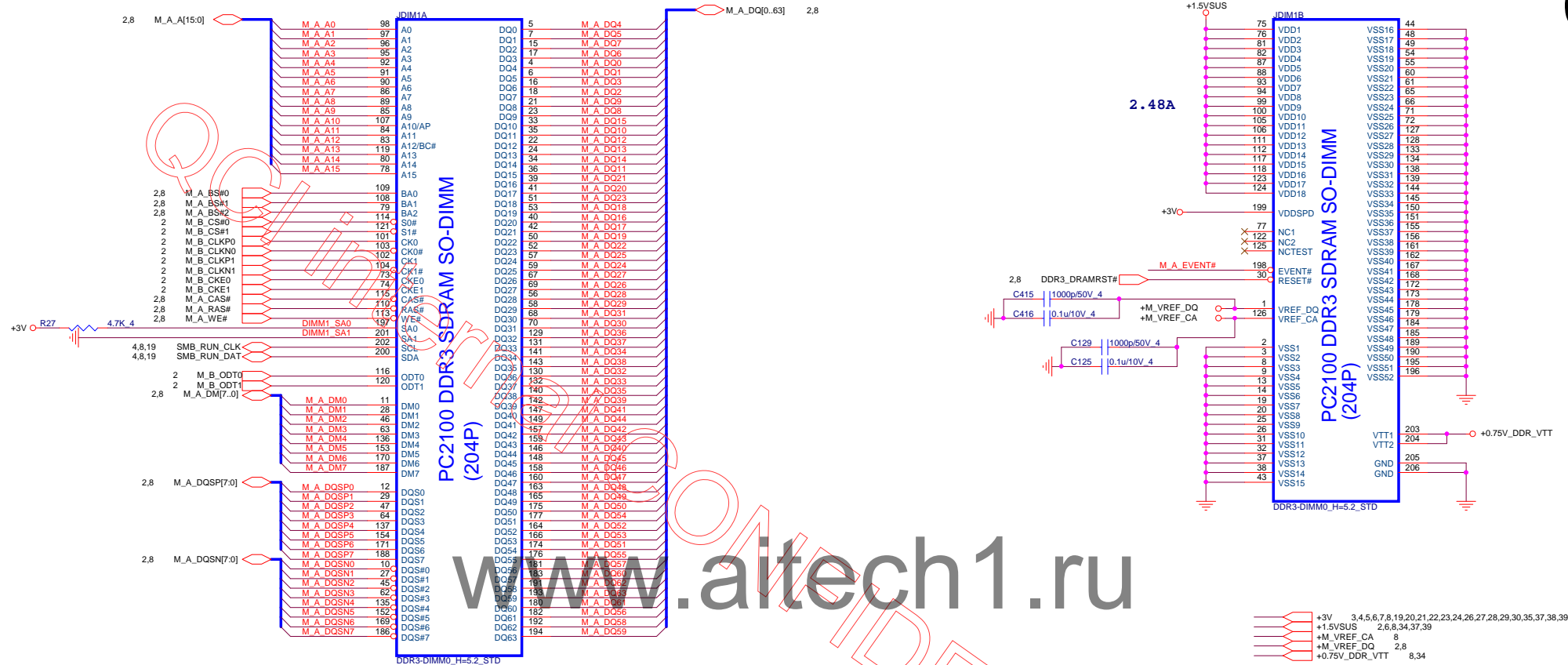
SYS_PWRGD

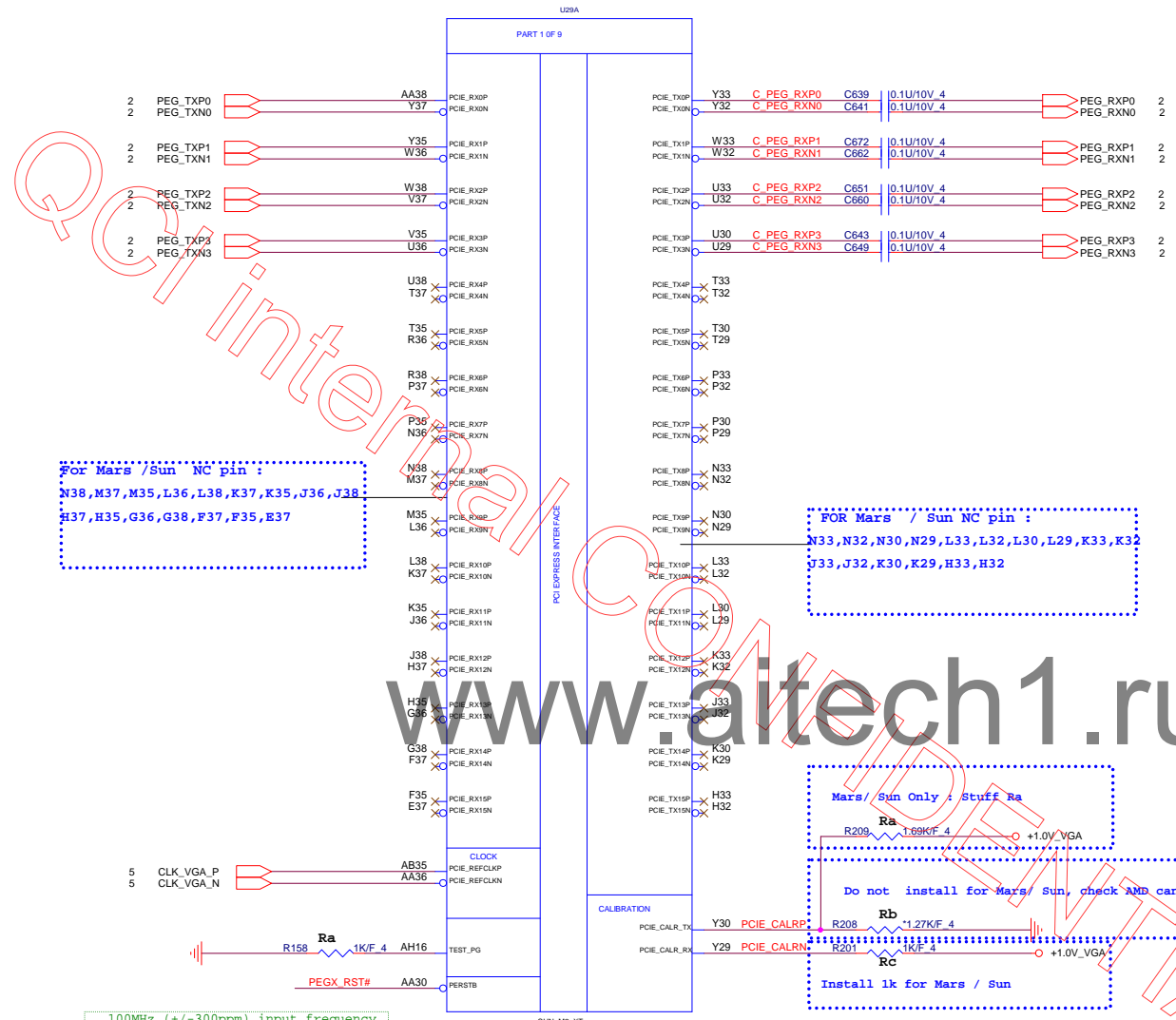


Modify for cost down

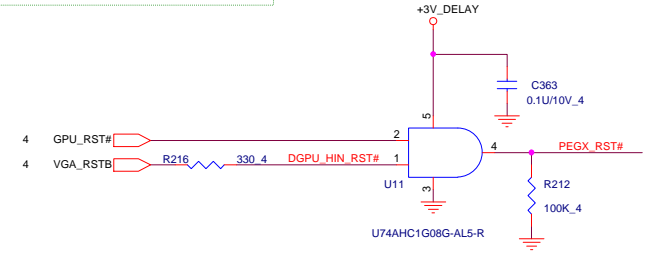
- +3V 3,4,5,6,8,9,19,20,21,22,23,24,26,27,28,29,30,35,37,38,39
- +3VS5 4,5,6,22,29,30,32,33,37,39
- +1.8VS5 4,6,33,34,35,37,39

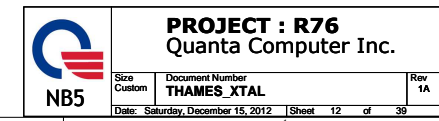


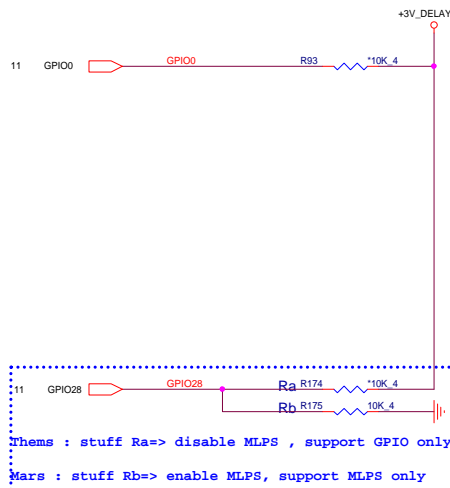
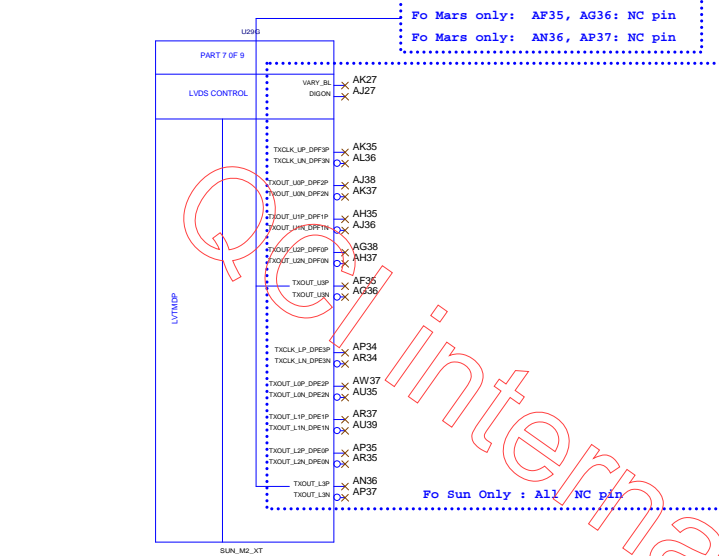




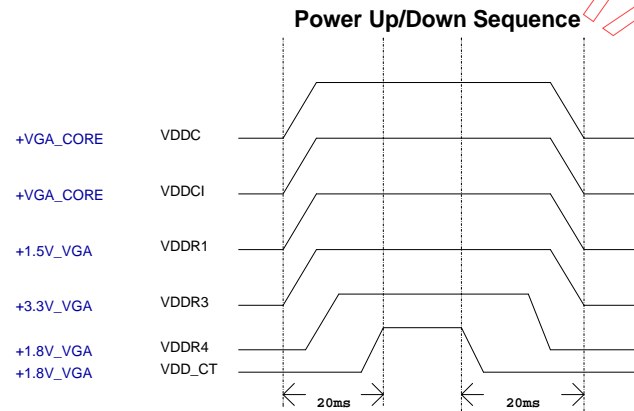
	MARS	
Ra	1.69K	
Rb	n/a	
Rc	1K	







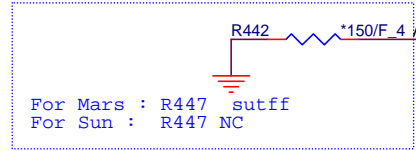
CONFIGURATION STRAPS -- SEE EACH STRAP FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET																						
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting																		
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X																		
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X																		
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X																		
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1																		
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0																		
ROMIDCFG2[0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type <table><tr><td>100 - 512Kbit</td><td>M25P60</td><td>(SD)</td></tr><tr><td>101 - 1Mbit</td><td>M25P60</td><td>(SD)</td></tr><tr><td>100 - 2Mbit</td><td>M25P60</td><td>(SD)</td></tr><tr><td>101 - 2Mbit</td><td>M25P60</td><td>(SD)</td></tr><tr><td>100 - 8Mbit</td><td>M25P60</td><td>(Chingis)</td></tr><tr><td>101 - 1Mbit</td><td>Pm25LV010</td><td>(Chingis)</td></tr></table>	100 - 512Kbit	M25P60	(SD)	101 - 1Mbit	M25P60	(SD)	100 - 2Mbit	M25P60	(SD)	101 - 2Mbit	M25P60	(SD)	100 - 8Mbit	M25P60	(Chingis)	101 - 1Mbit	Pm25LV010	(Chingis)	XXX
100 - 512Kbit	M25P60	(SD)																				
101 - 1Mbit	M25P60	(SD)																				
100 - 2Mbit	M25P60	(SD)																				
101 - 2Mbit	M25P60	(SD)																				
100 - 8Mbit	M25P60	(Chingis)																				
101 - 1Mbit	Pm25LV010	(Chingis)																				
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X																		
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX																		
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X																		
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0																		
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX																		

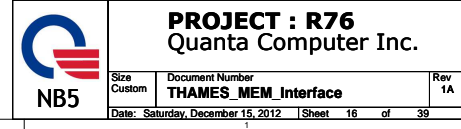




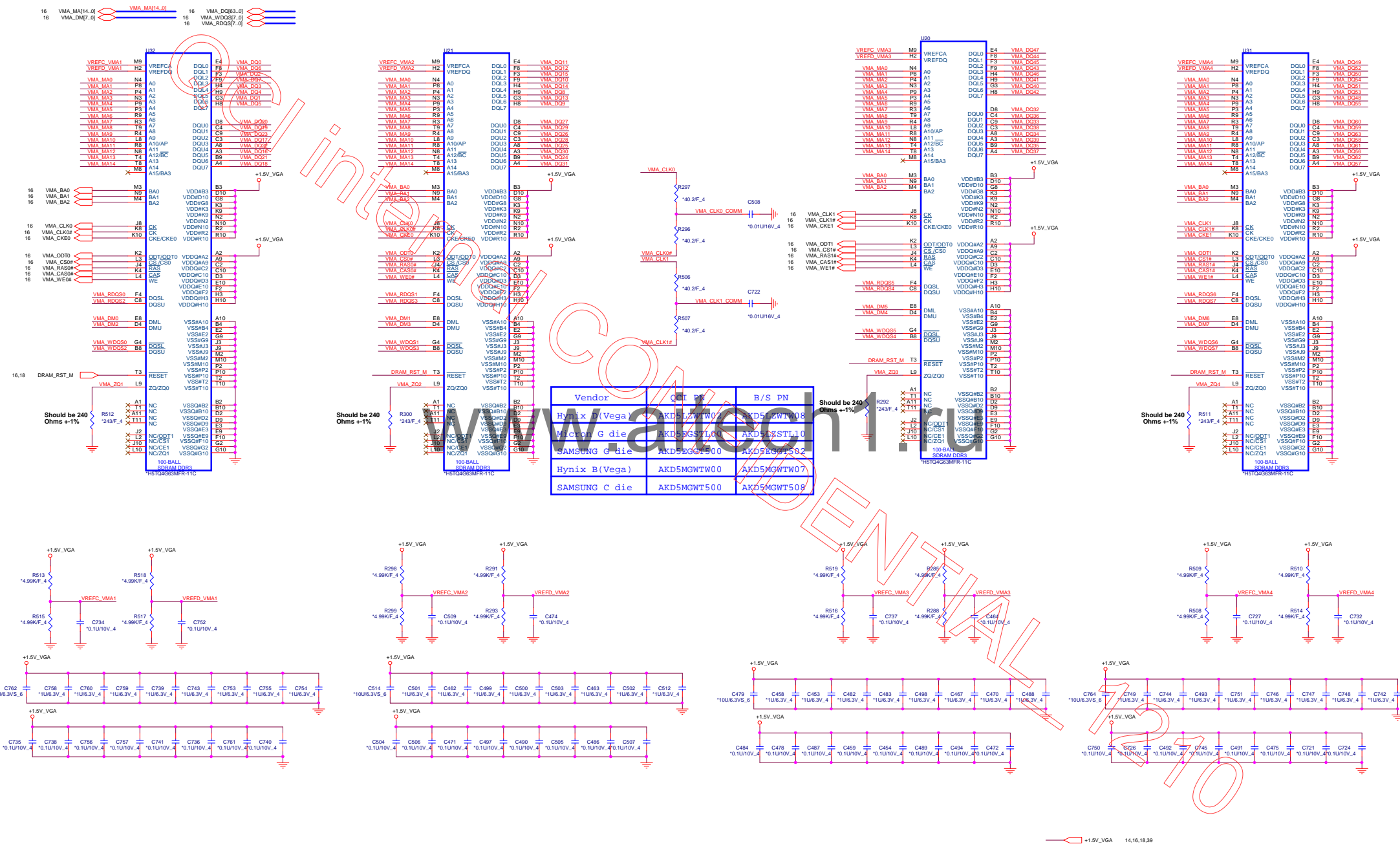
2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

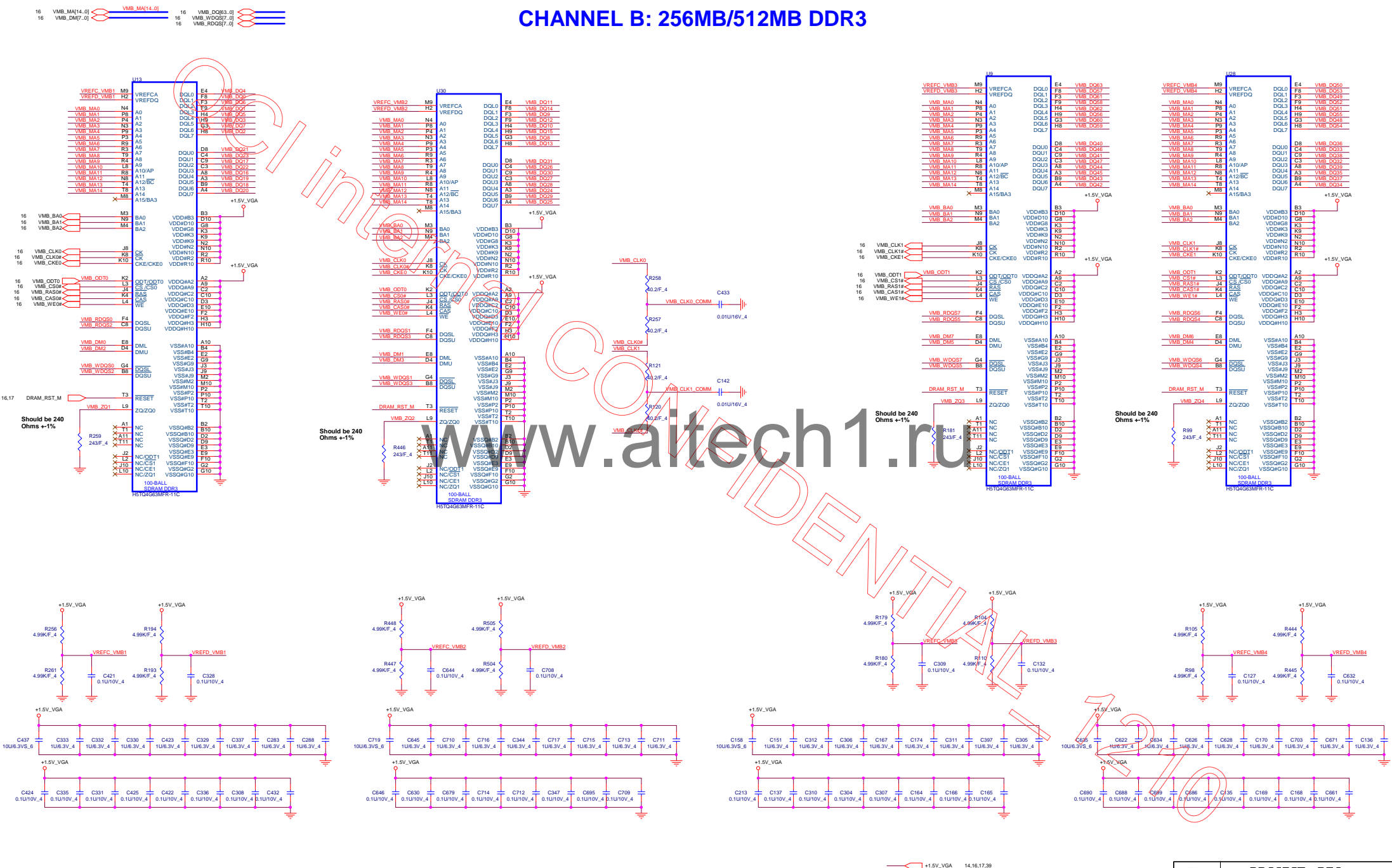
PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

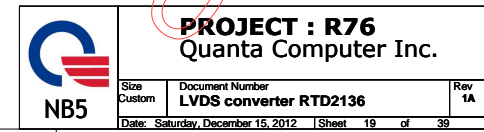




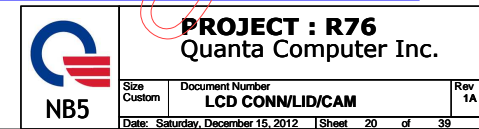
CHANNEL A: 256MB/512MB DDR3



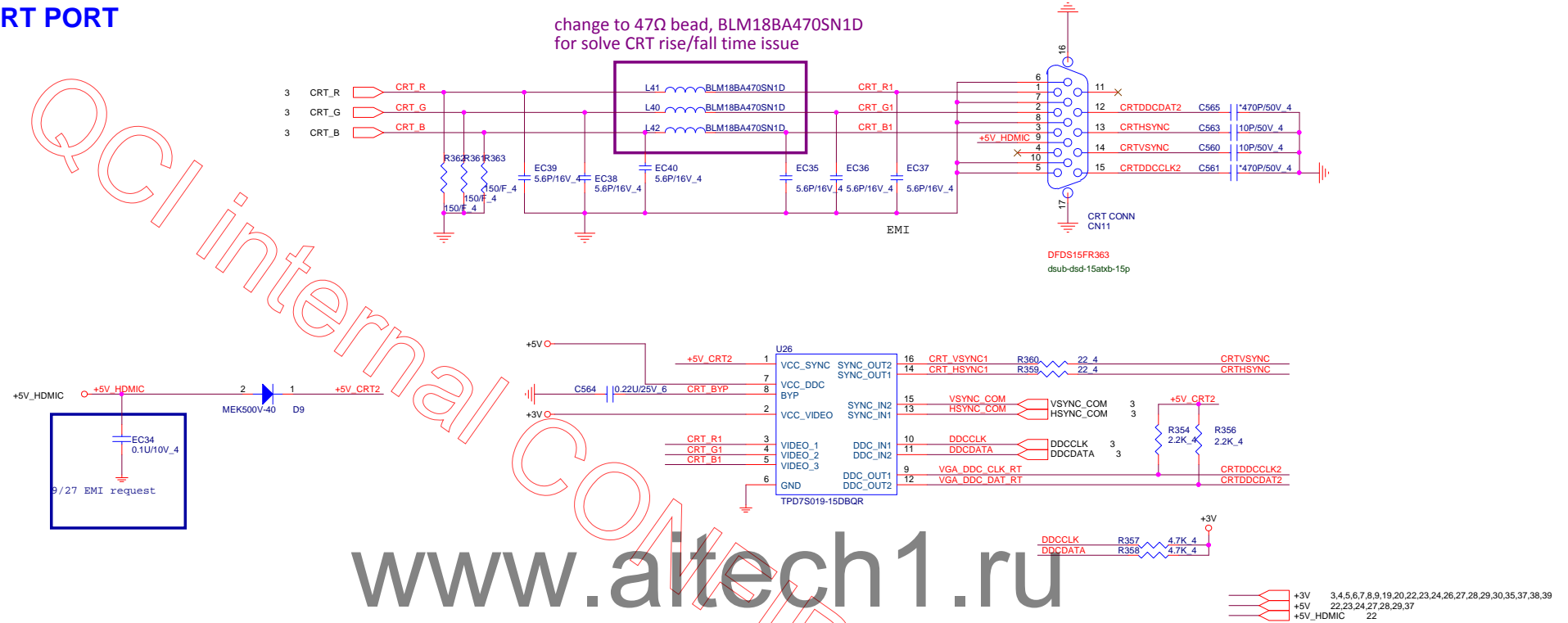




20



CRT PORT



HOLE

HOLE

FAN hole

CPU BKT

VGA BKT

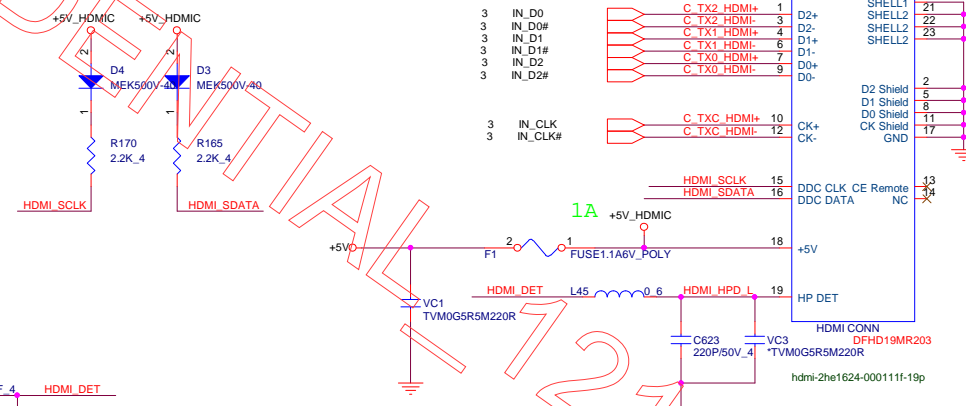
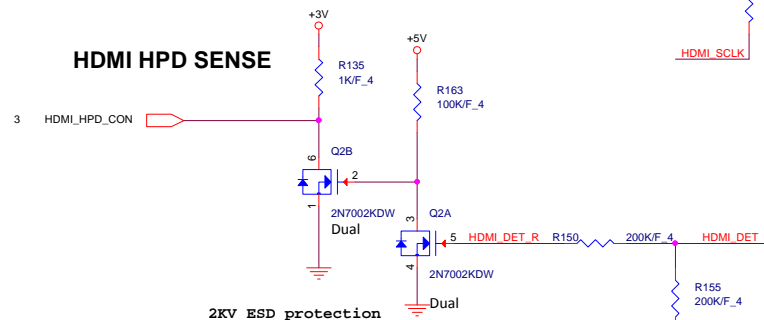
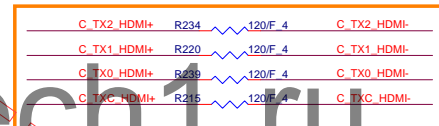
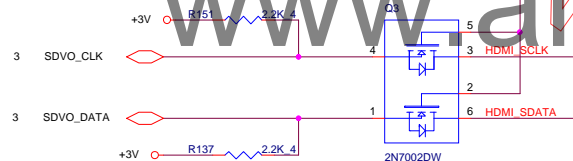
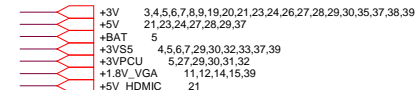
THERMAL BKT

KB lock

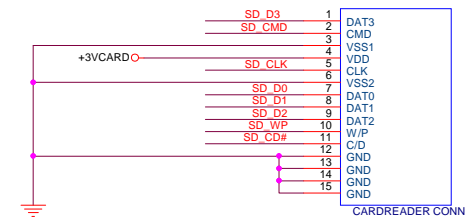
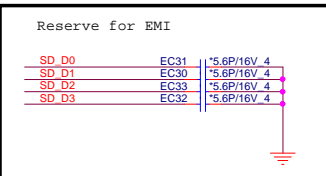


PROJECT : R76
Quanta Computer Inc.

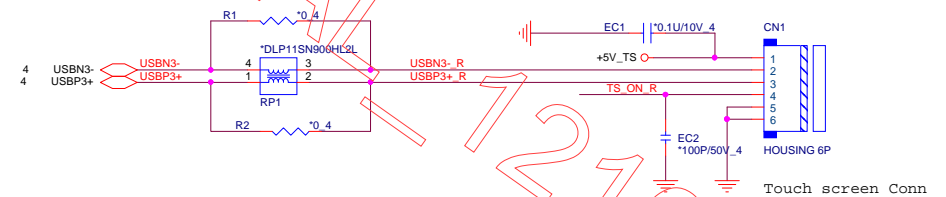
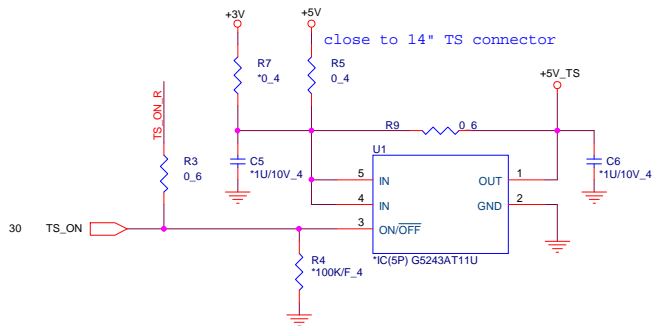
Size Custom	Document Number CRT,Hole	Rev 1A
Date: Saturday, December 15, 2012		Sheet 21 of 39

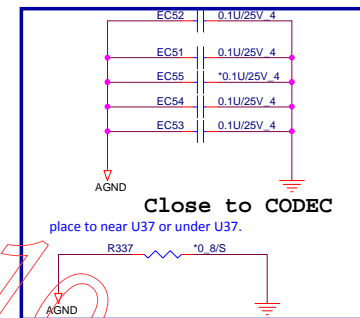
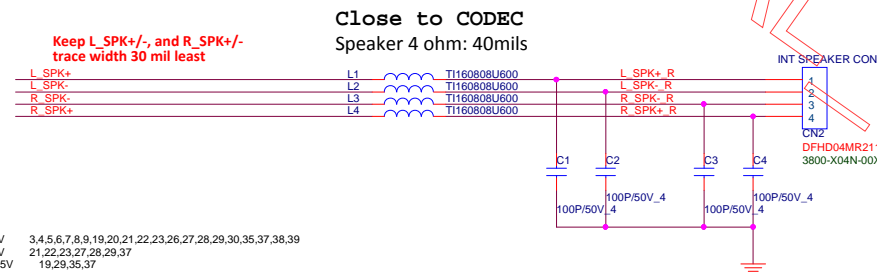
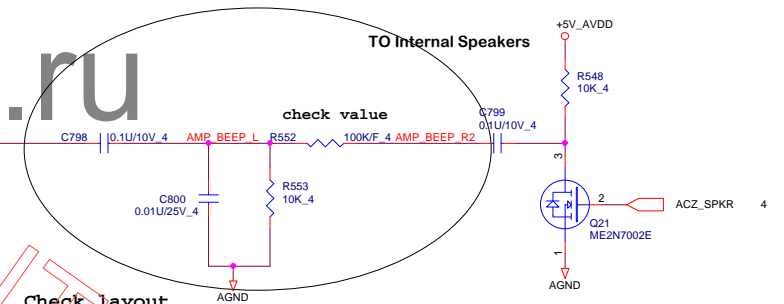
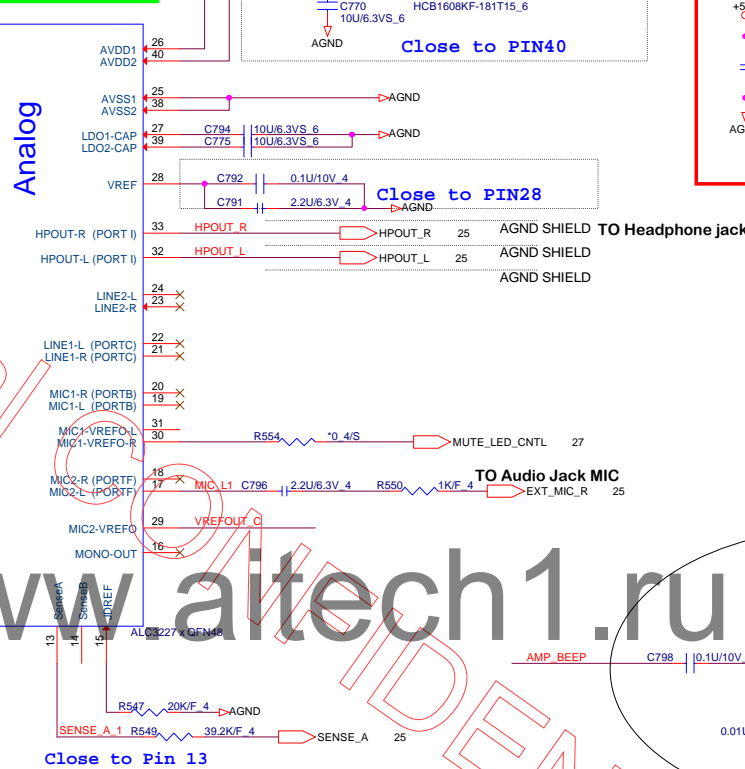
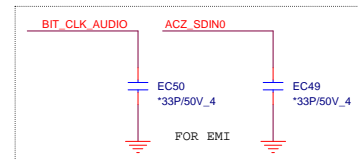
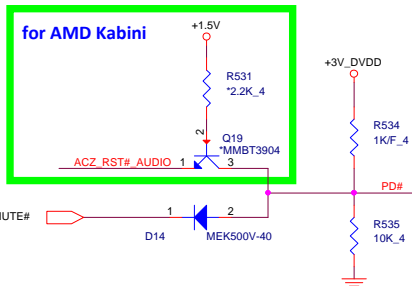
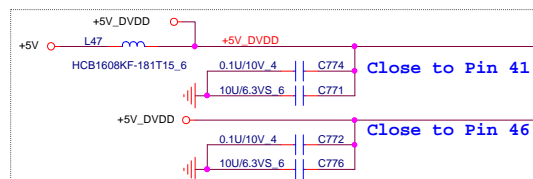
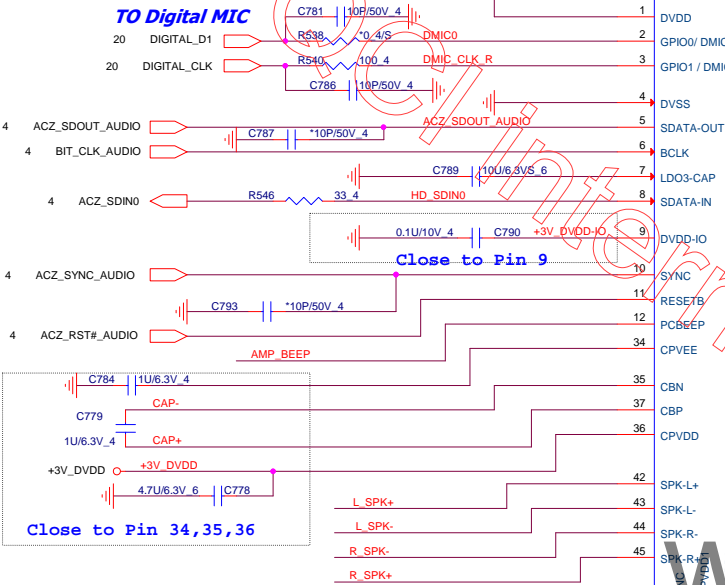
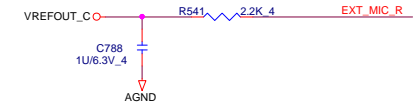
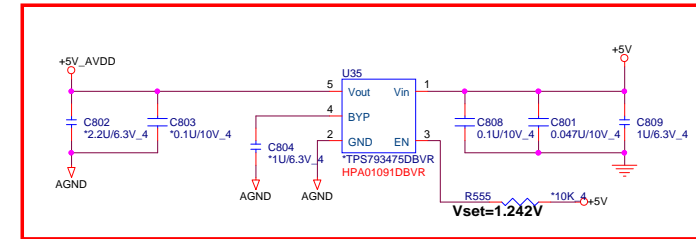
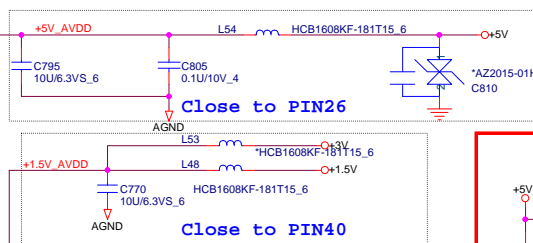
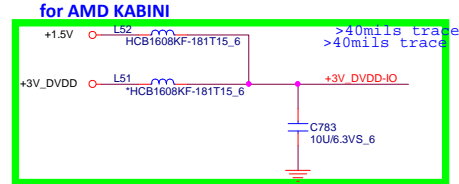
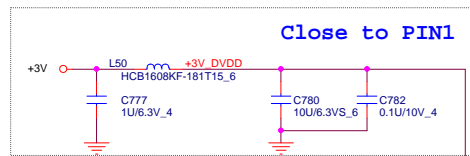


SP1	SD D1	
SP2	SD D0	MS D1
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

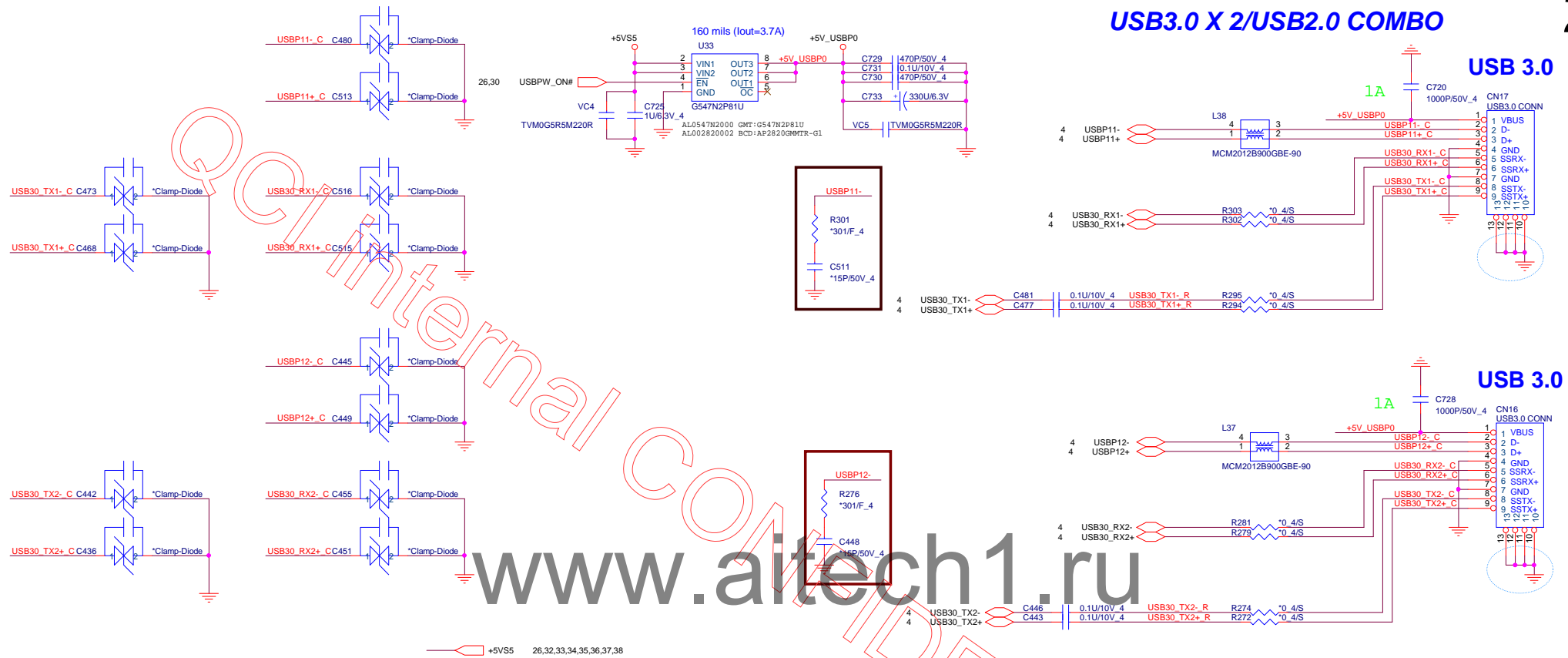


Change footprint to
sdcard-psdbtc-09glbs1nn4h3-11p

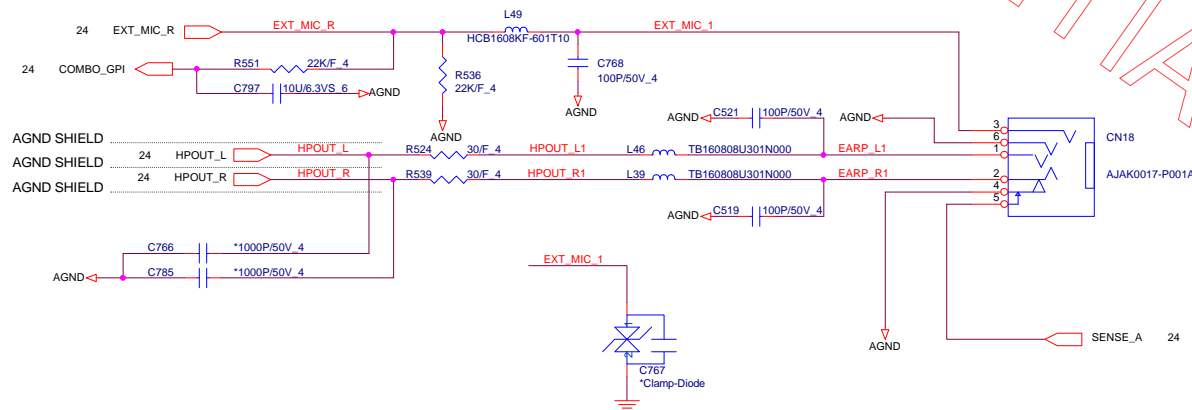




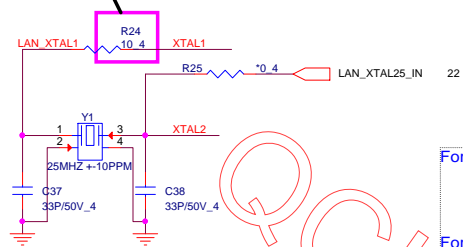
USB3.0 X 2/USB2.0 COMBO



COMBO JACK

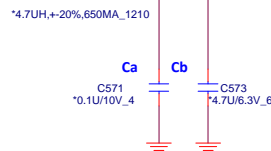
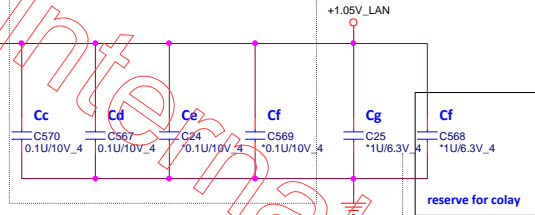
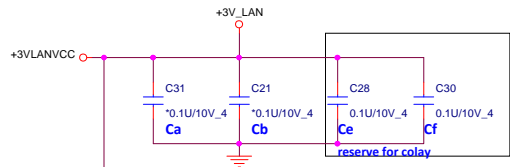
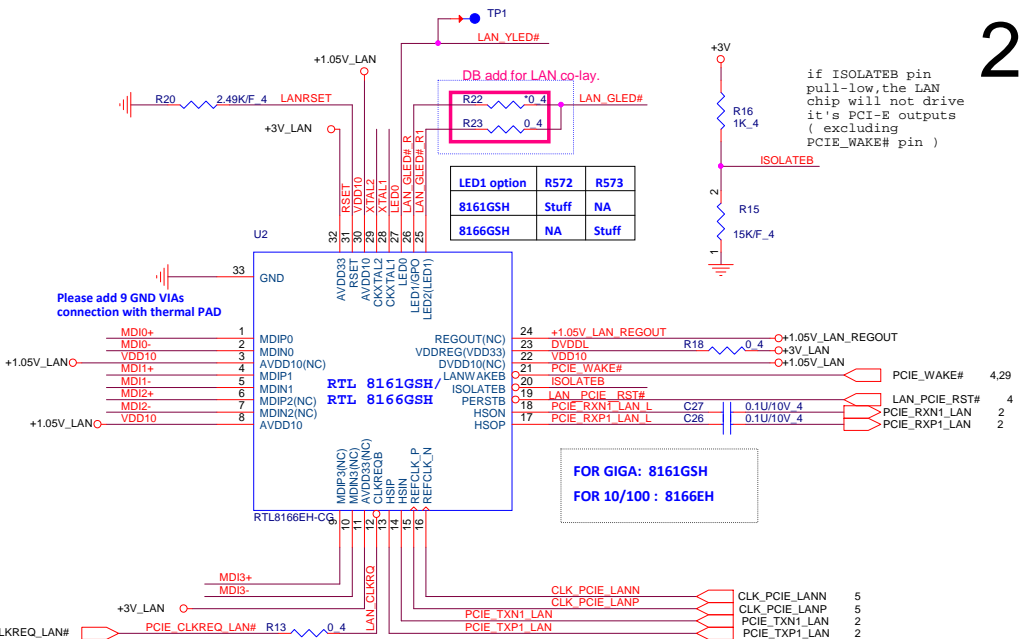


For EMI 0 ~ 22 ohm

Trace < 30 mil
Width > 60 mil
> 60 mil

Power trace Layout 宽度 > 60mil

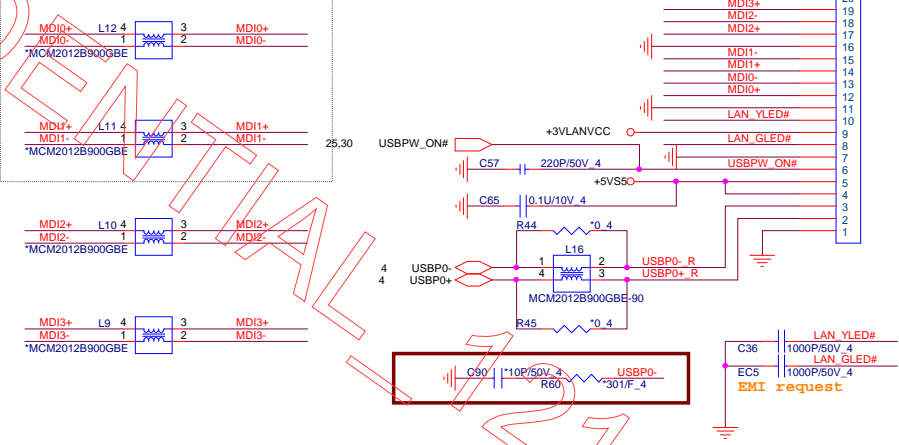
> 60mil

For GbE
Stuff La, Ca, CbFor 10/100
NA: La, Ca, CbFor GbE
* Place Cc, Cd, Ce, Cf
close to each VDD10 pin-- 3, 8, 22, 30For 10/100 NA Ce, Cf
* Place Cc, Cd
close to each VDD10 pin-- 8, 30 only.For GbE
* Place Cg close to each VDD10 pin-- 22 (reserve)For 10/100
* Place Cf close to each VDD10 pin-- 30 (reserve)For 10/100
* Stuff Ce and Cf only, close to each VDD33 pin-- 23, 32For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32* Place Cc and Cd close to each VDD33 pin-- 23, 32
For GIGA
Stuff Cc, Cd
For 10/100
NA: Cc, Cd
Remove For Not Using SWR mode+3V 3,4,5,6,7,8,9,19,20,21,22,23,24,27,28,29,30,35,37,38,39
+5VSS 25,32,33,34,35,36,37,38
+3VLANVCC 22,37FOR GIGA: 8161GSH
FOR 10/100: 8166EH

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LAN conn & Right SIDE USBX1

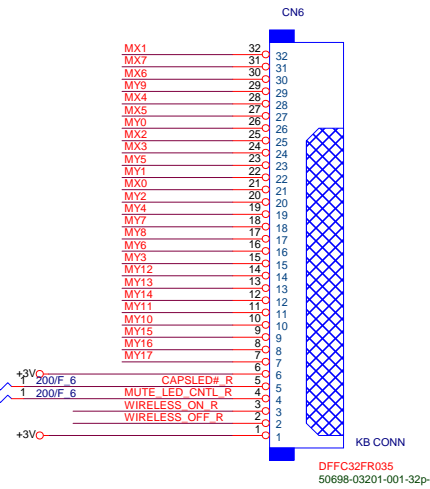
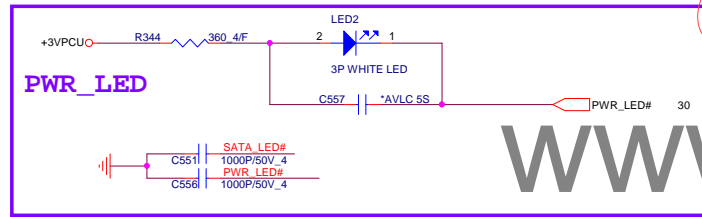
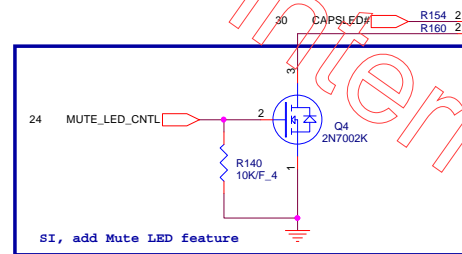
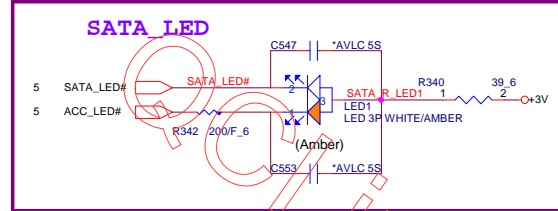
For 10/100 only

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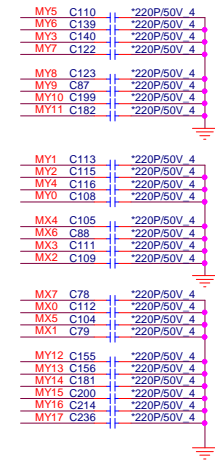
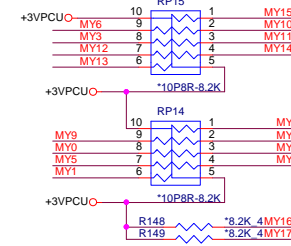
Size	Document Number	Rev
Custom	RTL 8105E/RJ45	1A

Date: Saturday, December 15, 2012 | Sheet 26 of 39

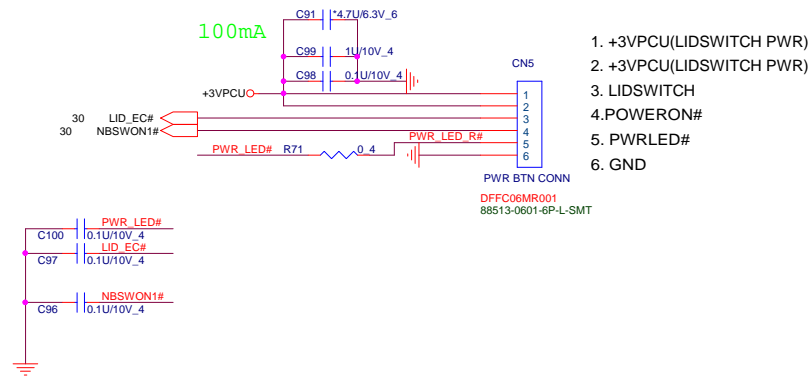
KEYBOARD Con.



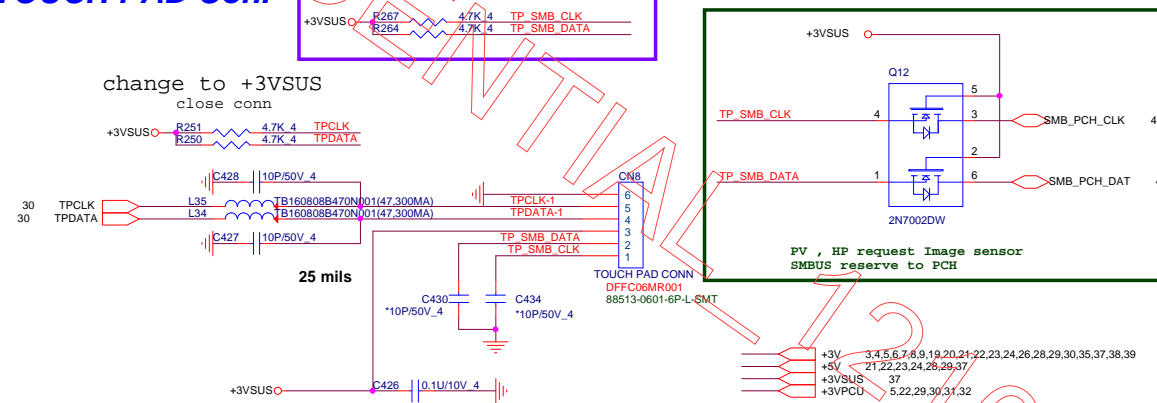
KEYBOARD PULL-UP



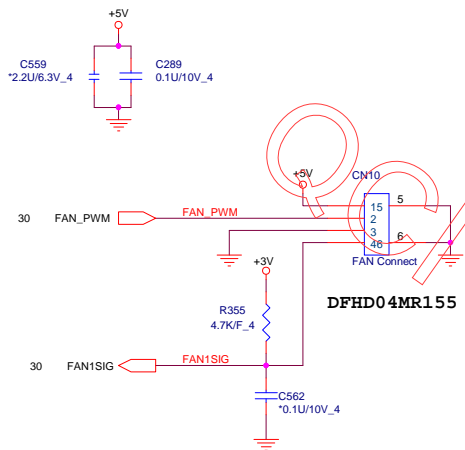
POWER BOTTON CONNECT



TOUCH PAD Con.

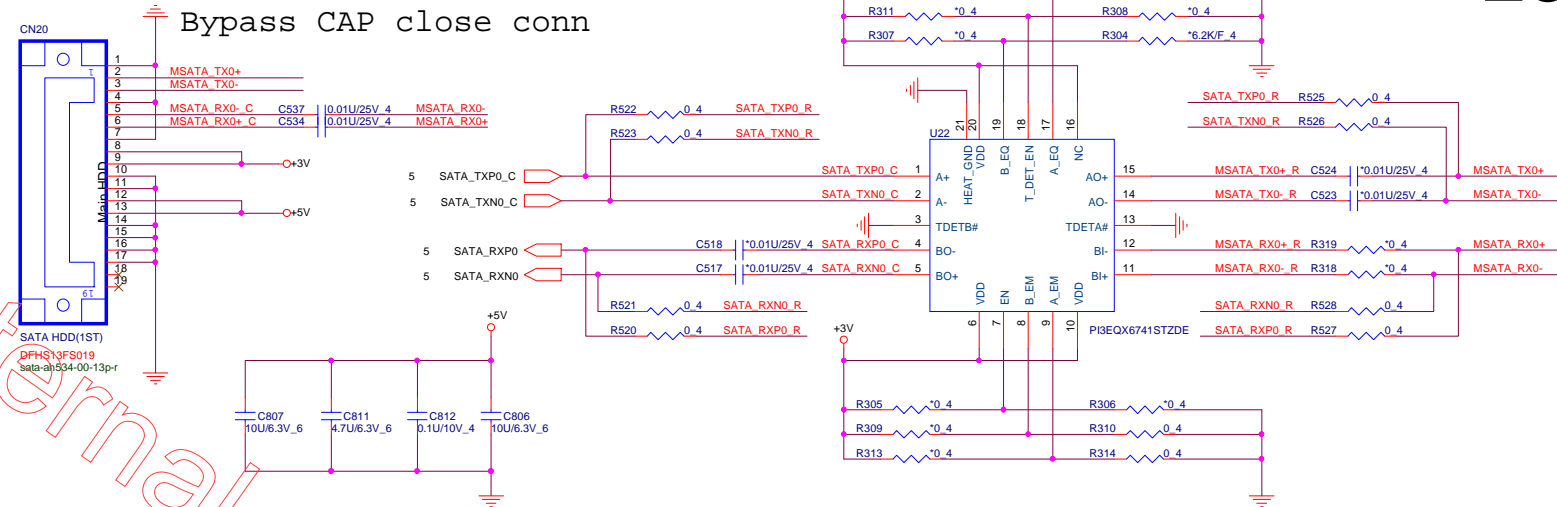


CPU FAN



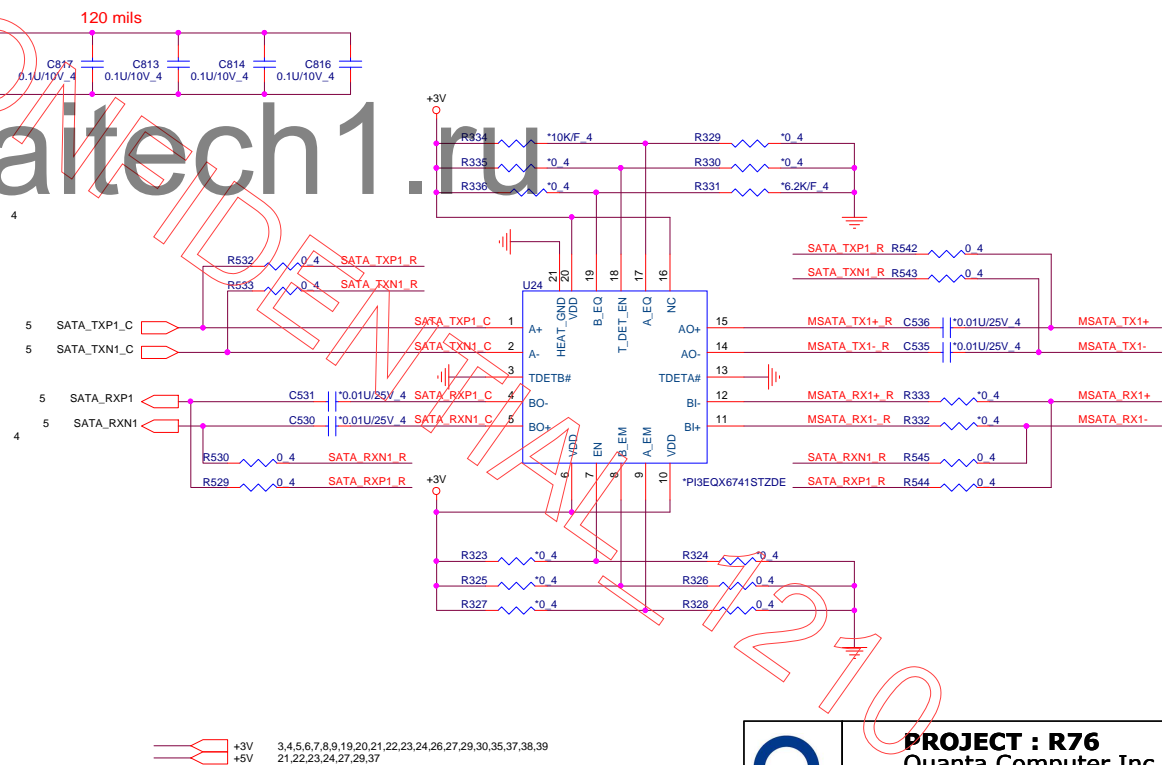
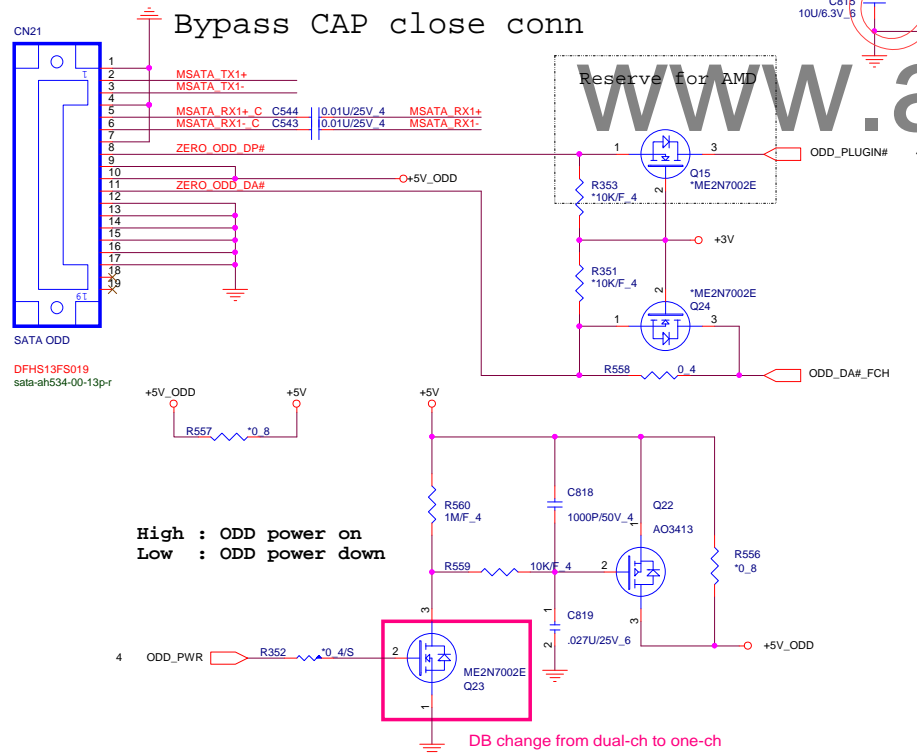
SATA HDD CONNECTOR

- Bypass CAP close conn

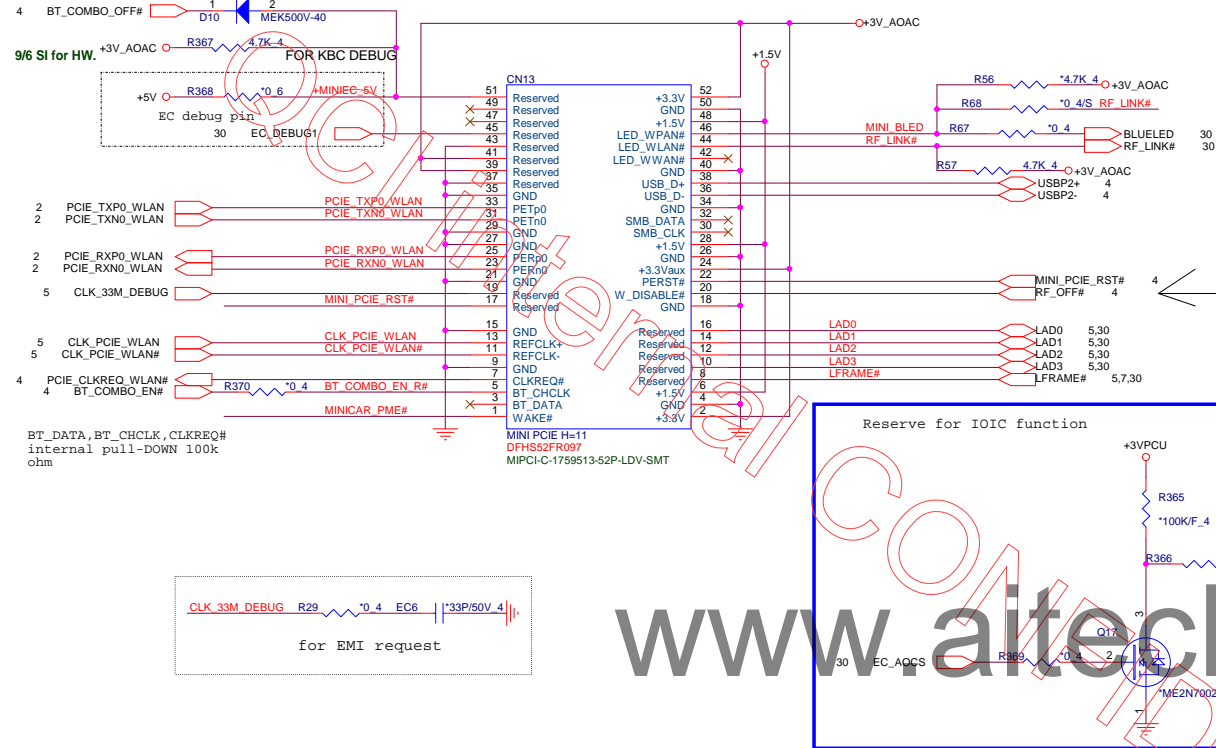


SATA ODD CONNECTOR

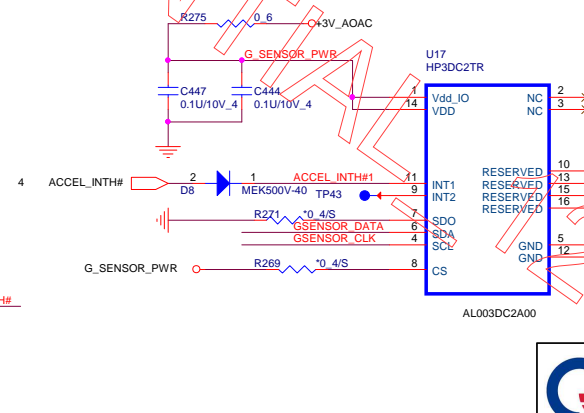
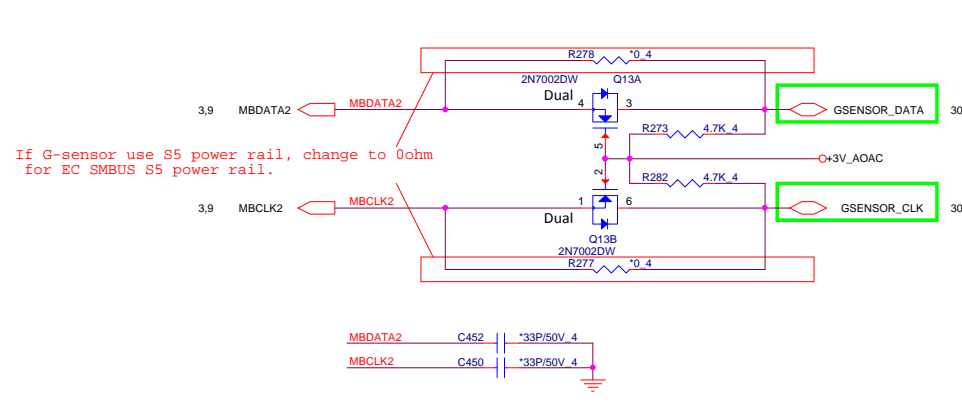
Bypass CAP close conn

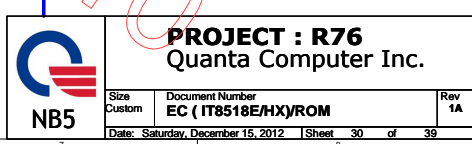


Mini PCI-E Card 1 WLAN

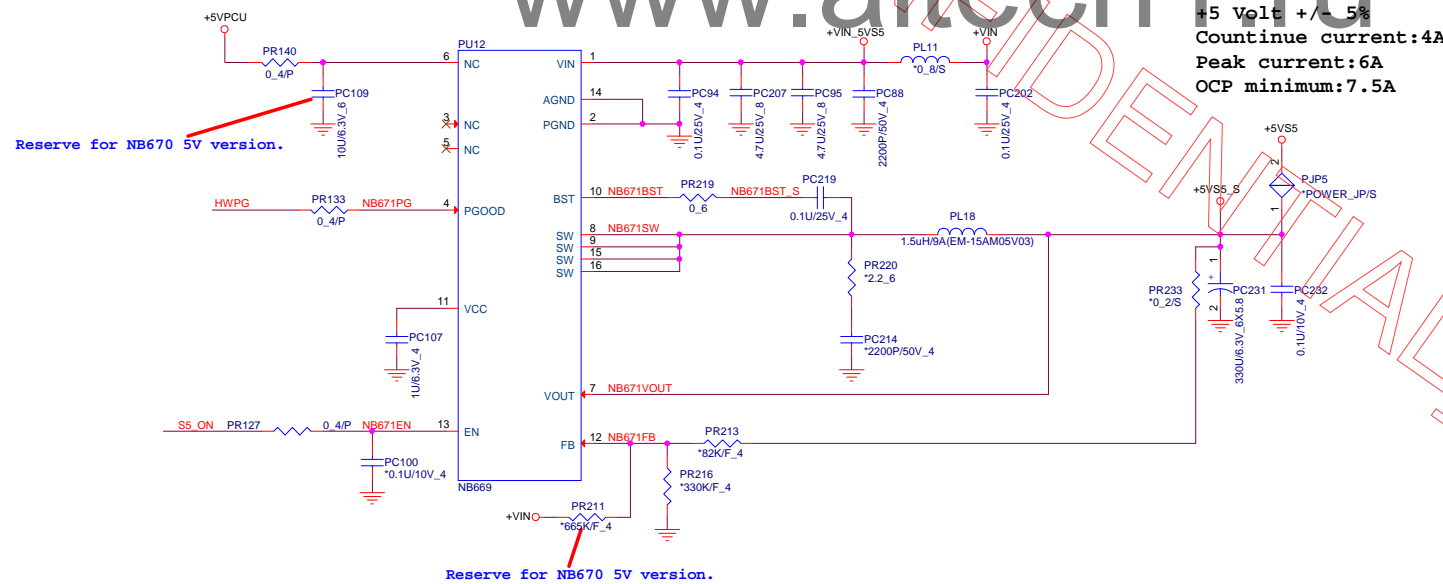
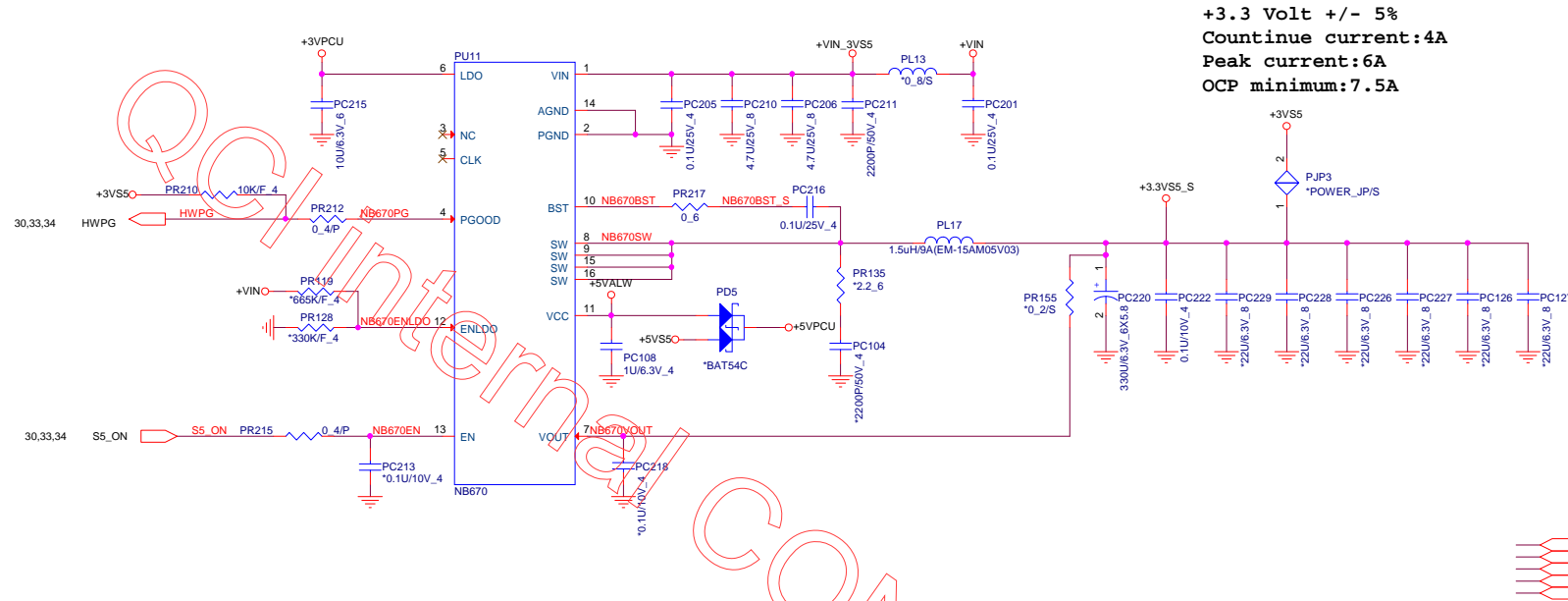


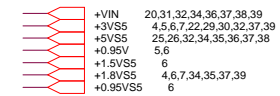
Accelerometer Sensor



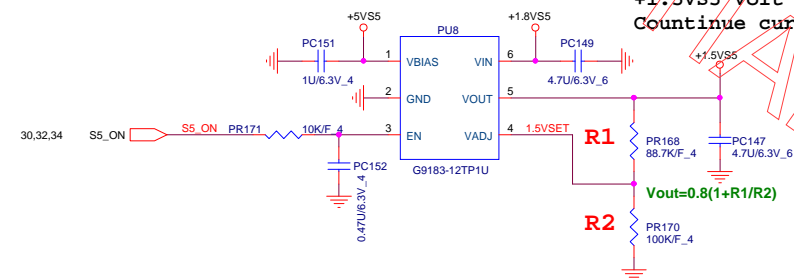
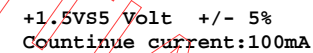


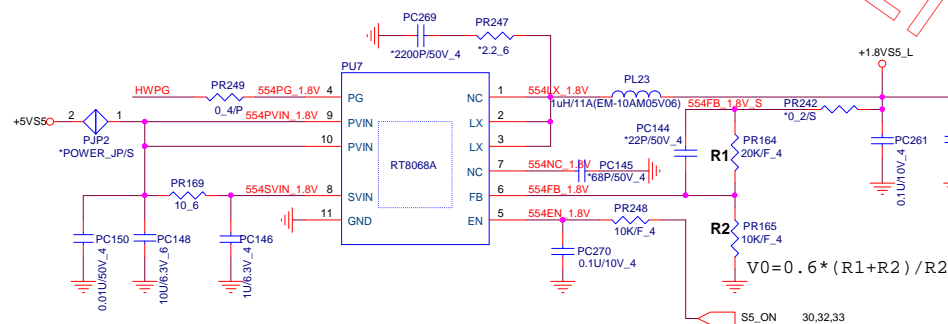
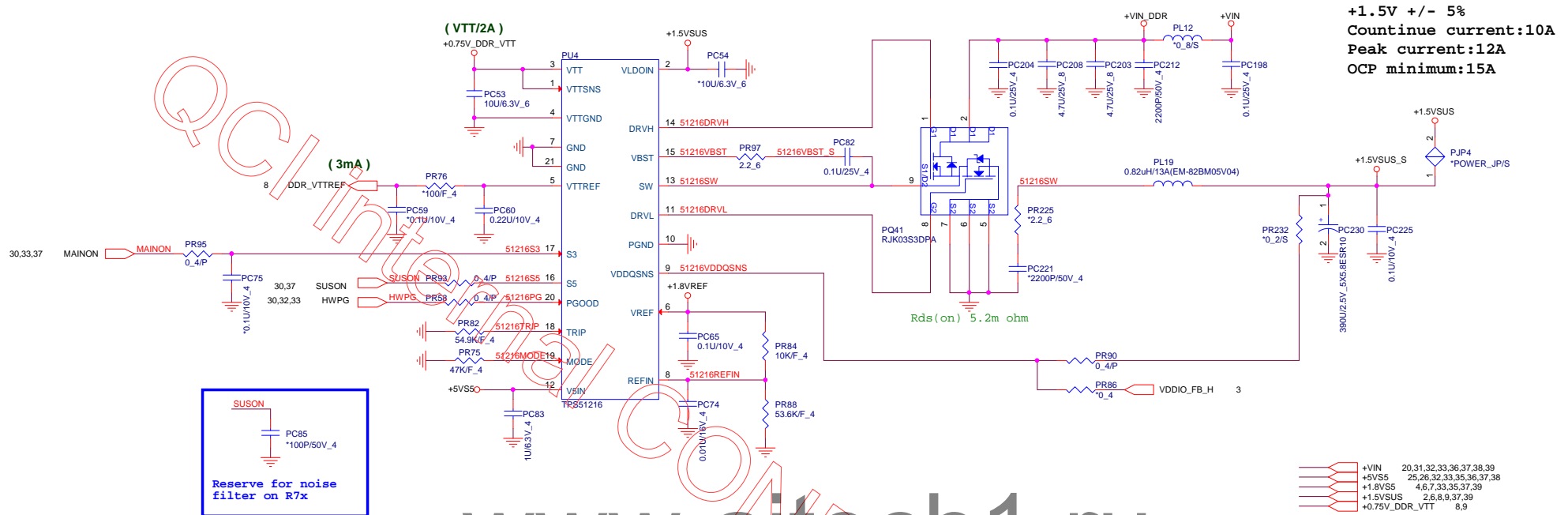


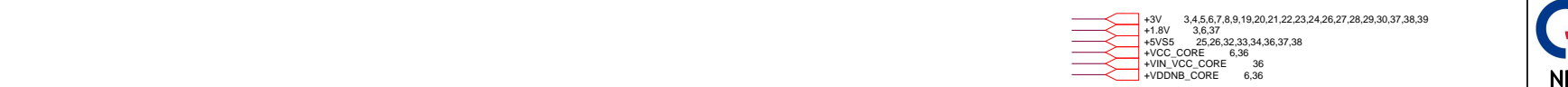




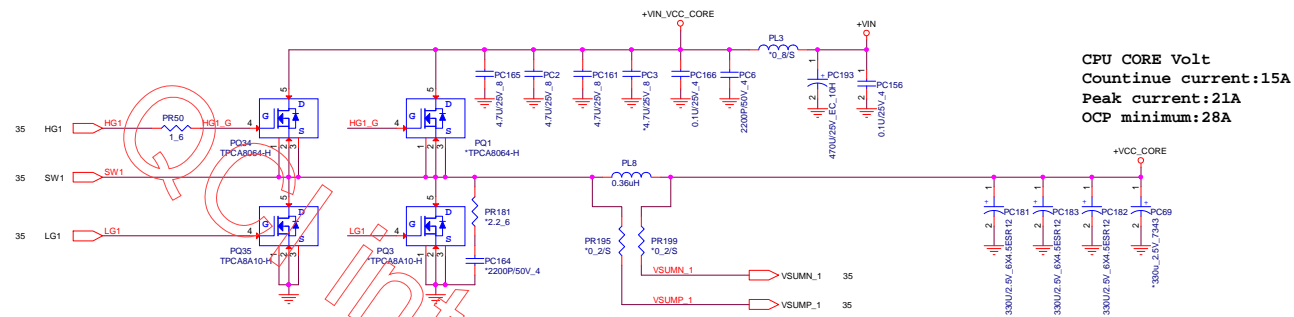
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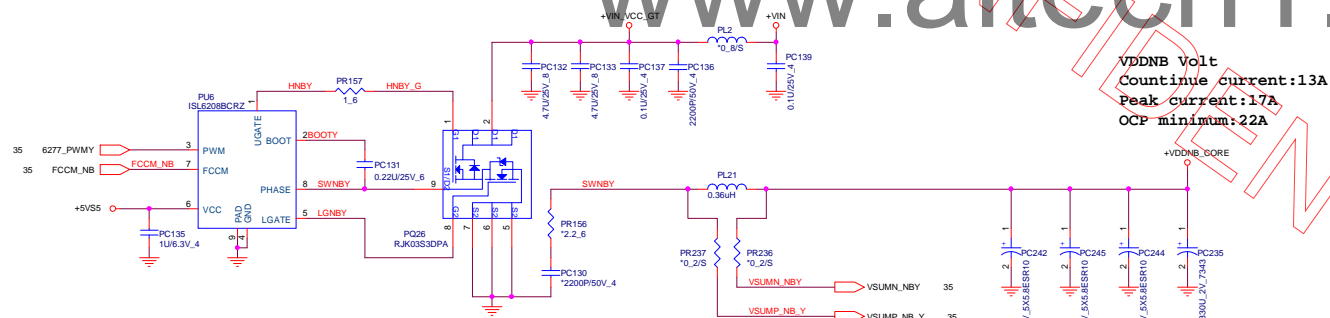


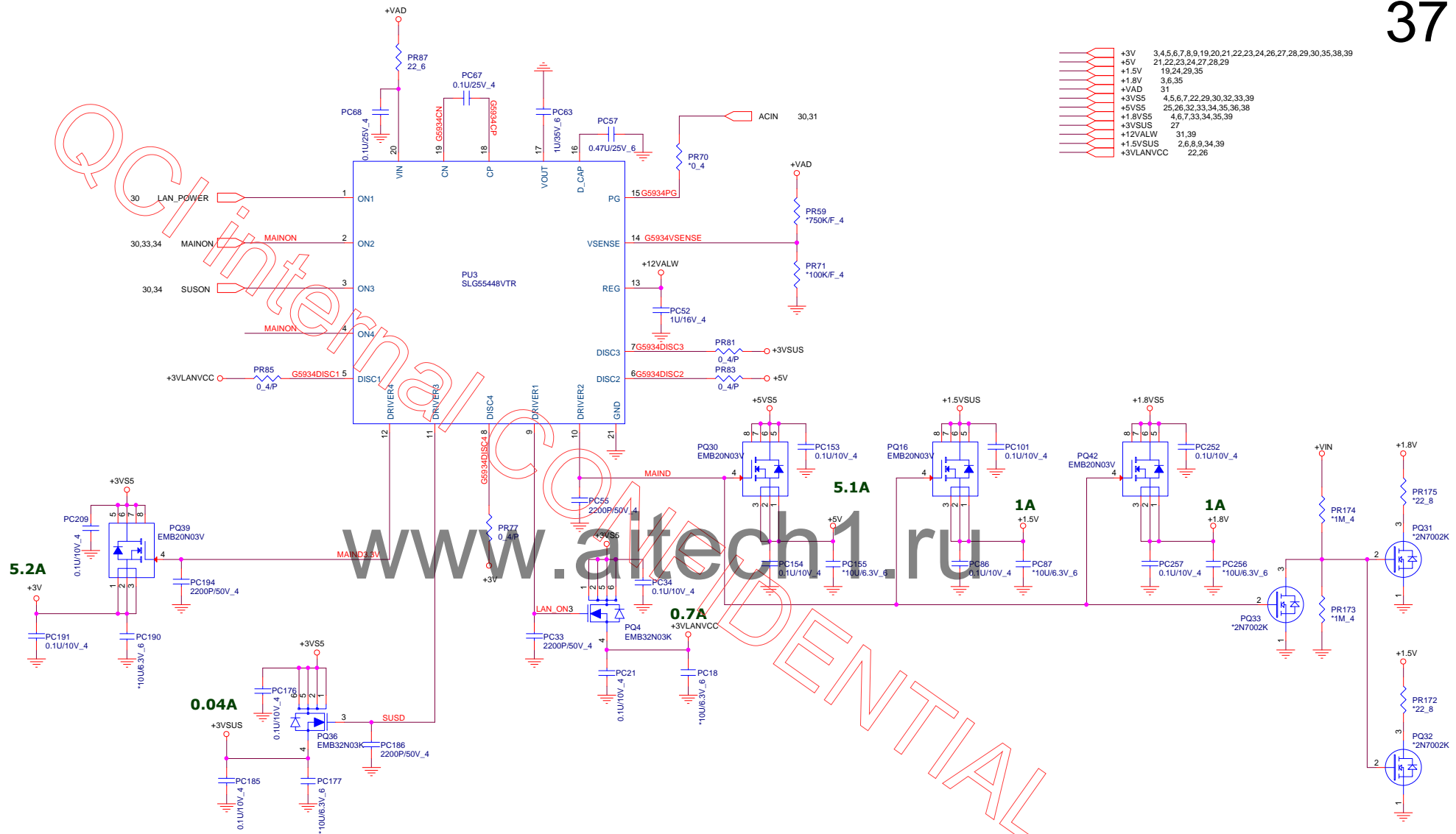
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+VIN 20,31,32,33,34,37,38,39
+VSS 25,26,32,33,34,35,37,38
+VCC_CORE 6,35
+VDDNB_CORE 6,35
+VIN_VCC_CORE 35

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GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V

Default

Mars (25W)

+VGA_CORE

Continue current: 25A

Peak current: 30A

OCP minimum: 33A

L-L: 0mV/A

11 DGPU_PROCHOT#

This NTC Close to Phase 1 MOSFET

PUS
NCP3218G

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DCR_1.4m ohm

DCR_1.4m ohm

Shortest the net trace

Close to Phase 1 Inductor

+3V	3,4,5,6,7,8,9,19,20,21,22,23,24,26,27,28,29,30,35,37,39
+VIN	20,31,32,33,34,36,37,39
+5VS5	25,26,32,33,34,35,36,37
+VGA_CORE	14,39

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Size Custom	Document Number +VGACORE (NCP3218G)	Rev 1A
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+0.95V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A

R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V

$$V0 = 0.6 * (R1 + R2) / R2$$

